Optimizing Performance and Reliability of GaN MOSFET Devices

Owing to a high critical electric field and high electron mobility, GaN based lateral Heterojunction Field Effect Transistors (HFETs) are sought after for high voltage power and RF applications. However the device reliability continues to be a critical challenge to be overcome before successful commercialization. In this work, different dielectrics deposited by Atomic Layer Deposition (ALD) have been investigated for improving the threshold voltage stability and dynamic reliability of AlGaN/GaN based Metal-Oxide-Semiconductor-HFETs (MOS-HFETs). This work includes a first-of-its-kind comprehensive analysis of electrical characterization techniques and physics-based models required to evaluate and recommend any dielectric for mitigating surface trapping phenomena in the gate stack or the access-regions. Comparing the efficacy of different methods for characterization of dielectric/AlGaN interface traps, it is found that the popular conductance method has a severely constrained detection limit when the AlGaN barrier offers high resistance to the de-trapping electrons. A capacitance-based method is immune to the issue of barrier resistance, but is still restrictive in its range. To improve the range and accuracy of trap detection, a novel pulsed-IV-based methodology is developed and demonstrated to be applicable for detecting both shallow and deep traps and implemented on evaluating different high-k and low-k ALD dielectrics. Using physics-based simulation models and experimental data, it is demonstrated that the leakage at the surface of the AlGaN, whether through the passivation dielectric bulk or the dielectric/AlGaN interface, must be minimized to restrict the formation of a “virtual gate” and minimize current collapse. It was also found that an optimal passivation dielectric must create a high density of shallow interface donor traps to quicken the de-trapping of electrons from the “virtual gate” and the recovery of the channel underneath. Combining simulation and experimental
results, an optimal set of ALD dielectrics for a reliable gate stack and access-region passivation regions, respectively, was determined and will be discussed. The effectiveness of the resulting optimal dual dielectric passivation stack in mitigating current collapse and ensuring contact isolation is also demonstrated.

Biographical Sketch:

Veena Misra is a Professor of Electrical and Computer Engineering at North Carolina State University and also an IEEE Fellow. She is also the Director of the National Science Foundation Nanosystems Engineering Research Center on Advanced Self-Powered of Integrated Sensors and Technologies (ASSIST). She received the B.S., M.S., and Ph.D. degrees in electrical engineering from North Carolina State University, Raleigh. After working at the Advanced Products Research and Development Laboratories, Motorola Inc., Austin, TX she joined the faculty of North Carolina State University in 1998. She has authored or coauthored over 170 papers in the areas of state-of-the-art wide bandgap GaN and SiC devices, low-power CMOS devices, alternative high-mobility substrates, nanoscale magnetics, and energy-harvesting. Dr. Misra was the recipient of the 2001 National Science Foundation Presidential Early CAREER Award, the 2011 Alcoa Distinguished Engineering Research Award, and 2007 Outstanding Alumni Research Award. She also served as the general chair of the 2012 IEEE International Electron Device Meeting.