Navitas

Breaking Speed Limits with GaN Power ICs

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The Need for Speed

Switching Frequency

Bulky, Heavy & Expensive

Small, Light & Lower Cost

Efficiency

Today

Tomorrow

100kHz

1MHz

10MHz

Switching Frequency

Navitas
What is Slowing Us Down?

- Drivers
- EMI
- Sync
- REC
- Thermal
- Switch
- Magnetcs
- Topology
- Packaging
- Controller
- Silicon Limit
- 100kHz

Navitas
Wide Bandgap (WBG) Devices: Physics Drives Switch Performance

- WBG GaN material allows high electric fields so high carrier density can be achieved
- Two dimensional electron gas with AlGaN/GaN heteroepitaxy structure gives very high mobility in the channel and drain drift region
- Lateral device structure achieves extremely low $Q_g$ and $Q_{OSS}$ and allows integration

![Diagram of GaN HEMT structure](image)

![Graph showing carrier mobility and EBR field for Si, 4H-SiC, and GaN](graph)

- **Mobility (cm$^2$/Vs)**
- **EBR Field (MV/cm)**

Si | 4H-SiC | GaN
Speed Limit?
Can Magnetics Rise to the Speed Challenge?

- Boundaries vary with material, DC/AC current mix, power, etc.
- Majority of mass production applications run 65kHz – 150kHz
- 5x frequency increase is within today’s capability
Removing speed limits:

High Frequency Magnetics “GaN Optimized”

N59 optimized for 2MHz

3F & 4F up to 10MHz
**Breaking Speed Limits:**

650V Navitas eMode GaN at 27MHz & 40MHz

**Class Phi-2 DC/AC converter: Stanford / Navitas demo**

- 50% less loss than RF Si
- 16x smaller package
- Air-core inductors
- Minimal FET loss
- Negligible gate drive loss

<table>
<thead>
<tr>
<th>Technology</th>
<th>V</th>
<th>Pack (mm)</th>
<th>FSW (MHz)</th>
<th>Eff. (%)</th>
<th>Power (W)</th>
</tr>
</thead>
<tbody>
<tr>
<td>RF Si (ARF521)</td>
<td>500</td>
<td>M174 22x22</td>
<td>27.12</td>
<td>91%</td>
<td>150</td>
</tr>
<tr>
<td>eMode GaN</td>
<td>650</td>
<td>QFN 5x6</td>
<td>27.12</td>
<td>96%</td>
<td>150</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>40.00</td>
<td>93%</td>
<td>115</td>
</tr>
</tbody>
</table>

- 27.12MHz, φ2 Inverter, VDS of GaN
- 20ns/div, 150V/div
Speed Limit: Existing GaN Packages

Slow, Expensive, Non-Standard

- **Through-hole**
  - High inductance, limits switching frequency

- **Cascode** (co-pack and/or stacking)
  - Multi-die, additional components
  - Higher cost for dice and assembly

- **PCB-embedded**
  - Non-standard, high cost
Removing Speed Limits:
Fast, Low Cost, Industry-Standard QFN

• Leadframe-based 5X6mm power package outline
• Low profile, small footprint with HV clearance
• Kelvin source connection for gate drive return
• Low inductance power connections (~0.2nH)
• Low thermal resistance (<2°C/W)
• I/O pins enough for drive functions
• High volume
• Reliable
• Low cost
Speed Limit:
Complex Drive

- dMode GaN needs extra FET, extra passives, isolation, complex packaging
- Early eMode GaN requires many added circuits:

Ref: GaN Systems Application note GN001 Rev 2014-10-21

Slow it down to protect gate from spikes! Some even recommend to add a Zener and ferrite bead.
Creating the World’s First allGaN™ Power ICs

Fastest, most efficient GaN Power FETs

iDrive First & Fastest Integrated GaN Gate Driver

World’s First allGaN™ Power IC

Up to 40MHz switching, 4x higher density & 20% lower system cost
Removing Speed Limits:

Navitas iDrive™ GaN Power IC

- **Monolithic** integration
- 20X lower drive loss than silicon
- Driver impedance matched to power device
- Shorter prop delay than silicon (10ns)
- Zero inductance turn-off loop
- Digital input (hysteretic)
- Rail-rail drive output
- Layout insensitive
Crisp & Efficient Gate Control

- Eliminates gate overshoot and undershoot
- Zero inductance on chip insures no turn-off loss

Discrete Driver & GaN FET

Monolithic GaN IC

20ns/div, 2V/div

$V_{GS}$
Removing Speed Limits: Topology

Hard-Switched

*Primary Switch Power Loss:*

\[ P_{\text{FET}} = P_{\text{COND}} + P_{\text{DIODE}} + P_{\text{T-ON}} + P_{\text{T-OFF}} + P_{\text{DR}} + P_{\text{QRR}} + P_{\text{QOSS}} \]
Removing Speed Limits: Topology

Hard-Switched → Soft-Switched

Primary Switch Power Loss:

\[ P_{\text{FET}} = P_{\text{COND}} \times k + P_{\text{DIODE}} + P_{\text{T-ON}} + P_{\text{T-OFF}} + P_{\text{DR}} + P_{\text{QRR}} + P_{\text{QOSS}} \]

- k-factor >1 due to increased circulating current, duty cycle loss
- \( P_{\text{T-On}} \) = 0 (soft-switch)
- \( P_{\text{Qoss}} \) ↓2-3X (silicon devices can have high Coss charging/discharging losses)
Removing Speed Limits: Topology & Switch

Hard-Switched → Soft-Switched with eMode GaN

**Primary Switch Power Loss:**

\[
P_{\text{FET}} = P_{\text{COND}} * k + P_{\text{DIODE}} + P_{\text{T-ON}} + P_{\text{T-OFF}} + P_{\text{DR}} + P_{\text{QRR}} + P_{\text{QOSS}}
\]

- **k-factor** >1 due to increased circulating current, duty cycle loss
- **\(P_{\text{T-On}}\)** = 0 (soft-switch)
- **\(P_{\text{Qoss}}\)** ↓ 10X 2-3X (GaN Coss charging/discharging loss negligible up to 2Mhz)
- **\(P_{\text{DRIVER}}\)** ↓ 10X (GaN \(P_{\text{DR}}\) negligible up to 2Mhz)
- **\(P_{\text{QRR}}\)** = 0
- **\(P_{\text{DIODE}}\)** ↓ 2X (reverse conduction loss reduced by synchronous rectification)
- **\(P_{\text{T-OFF}}\)** = Reduced (limited by I-V crossover loss due to drive loop impedance)
Removing Speed Limits: Topology & Switch & Integration

Hard-Switched $\rightarrow$ Soft-Switched with GaN Power IC

Primary Switch Power Loss:

$$P_{FET} = P_{COND} \ast k + P_{\text{DIOODE}} + P_{\text{T-ON}} + P_{\text{T-OFF}} + P_{\text{DR}} + P_{\text{QRR}} + P_{\text{QOSS}}$$

- $k$-factor $>1$ due to increased circulating current, duty cycle loss
- $P_{\text{T-On}} = 0$ (soft-switch)
- $P_{\text{Qoss}}$ $\downarrow 10X$ $2-3X$ (GaN Coss charging/discharging loss negligible up to 2Mhz)
- $P_{\text{DRIVER}}$ $\downarrow 10X$ (GaN $P_{\text{DR}}$ negligible up to 2Mhz)
- $P_{\text{QRR}} = 0$
- $P_{\text{DIOODE}}$ $\downarrow 3X$ $2X$ (synchronous rectification with improved deadtime control)
- $P_{\text{T-OFF}} = 0$ Reduced (near-zero drive loop impedance with integration)

$>10x$ frequency increase possible with higher efficiencies
No Bumps in the Road

EMI: Smooth, clean, controlled waveforms

- 500V Switching
- No overshoot / spike
- No oscillations
- ‘S-curve’ transitions
- ZVS Turn-on
- Zero Loss Turn-off
- Sync Rectification
- High frequency
- Small, low cost filter
Removing speed limits:

MHz Controllers ... with more, faster to come

PFC (BCM):
- L6562 (1MHz)
- NCP1608 (1MHz)
- UCC28061 (500kHz)

DC-DC (LLC):
- NCP1395 (1.2MHz)
- FAN7688 (500kHz) (+SR)
- ICE2HS01G (1MHz)

DC-DC (Sync Rectifier):
- NCP4305 (1MHz)
- UCC24610 (600kHz)

PWM:
- NCP1252 (500kHz)
- NCP1565 (1.5MHz)
- UCC28C44 (1MHz)
- UCC25705 (4MHz)

DSP:
- UCD3138 (2MHz)
- dsPIC33xx (5MHz)
- ADP1055 (1MHz)
Speed Limit?

Secondary Side SR FETs Get Better with GaN

- All relevant performance FOMs favor GaN at 60V
- $R_{DS(ON)} \times Q_G$ reflects drive losses
- $R_{DS(ON)} \times Q_{OSS}$ reflects turn-off losses with non-resonant rectification
- $R_{DS(ON)} \times Q_{RR}$ reflects stored minority carrier turn-off losses
  - Minimized with deadtime control
- Silicon FETs are in QFN5X6 packages, GaN is WLCSP

Note: Taken from datasheet typicals at 4.5/5V gate drive and capacitance curves
Speed test:
150W Boundary Conduction Mode (BCM) Boost PFC

- \(120V_{AC} = 167\text{-}230kHz\)
- \(220V_{AC} = 230\text{-}500kHz\)
- 265V peaks at 1MHz (L6562 \(F_{SW}\) max)

<table>
<thead>
<tr>
<th>Pack</th>
<th>Pack</th>
<th>(R_{DS(ON)}) m(\Omega)</th>
<th>(Q_G) nC</th>
<th>(C_{OSS,(er)}) pF</th>
<th>(C_{OSS,(tr)}) pF</th>
<th>(R^*Q_G) m(\Omega).nC</th>
<th>(R^*C_{OSS,(tr)}) m(\Omega).pF</th>
<th>(R^*C_{OSS,(er)}) m(\Omega).pF</th>
</tr>
</thead>
<tbody>
<tr>
<td>Navitas with iDrive(^{TM})</td>
<td>5x6</td>
<td>160</td>
<td>2.5</td>
<td>30</td>
<td>50</td>
<td>400</td>
<td>8,000</td>
<td>4,800</td>
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<tr>
<td>Si CP Series</td>
<td>8x8</td>
<td>180</td>
<td>32</td>
<td>69</td>
<td>180</td>
<td>5,760</td>
<td>32,400</td>
<td>12,400</td>
</tr>
<tr>
<td>Si C7 Series</td>
<td>8x8</td>
<td>115</td>
<td>35</td>
<td>53</td>
<td>579</td>
<td>4,025</td>
<td>66,600</td>
<td>6,100</td>
</tr>
<tr>
<td>GaN Benefits</td>
<td>&gt;50%</td>
<td>n/a</td>
<td>&gt;10x</td>
<td>&gt;2x</td>
<td>&gt;10x</td>
<td>&gt;10x</td>
<td>&gt;7x</td>
<td>&gt;2.5x</td>
</tr>
</tbody>
</table>

100 x 50 x 10mm with 2-layer, 2 oz Cu
No heatsinks, no forced air, no glue, potting or heat spreaders
• Si $C_{OSS}$ is 50x-100x worse than GaN at $V_{DS} < 30V$
• High loss due to large stored charge while hard-switching

120V$_{AC}$, Si CP partial hard-switching (~200kHz)

120V$_{AC}$, GaN clean ZVS waveforms (~200kHz)

• Turn-off losses are low due to powerful and parasitic-free drive integration with no overshoot
• Near loss-less ZVS turn-on transition
• Minimize deadtime for low reverse conduction loss
Speed Test:
Silicon Hits a Speed Bump ... and GaN Drives On

- ‘No heatsink’ design
- GaN runs cool
- Superjunction silicon FETs
  - Run 30-50°C hotter
  - Cannot deliver the power
  - Exhibit highly lossy resonant behavior
The Road Ahead…