Digital Vs. Analog Power Control for Microprocessor Core Regulation

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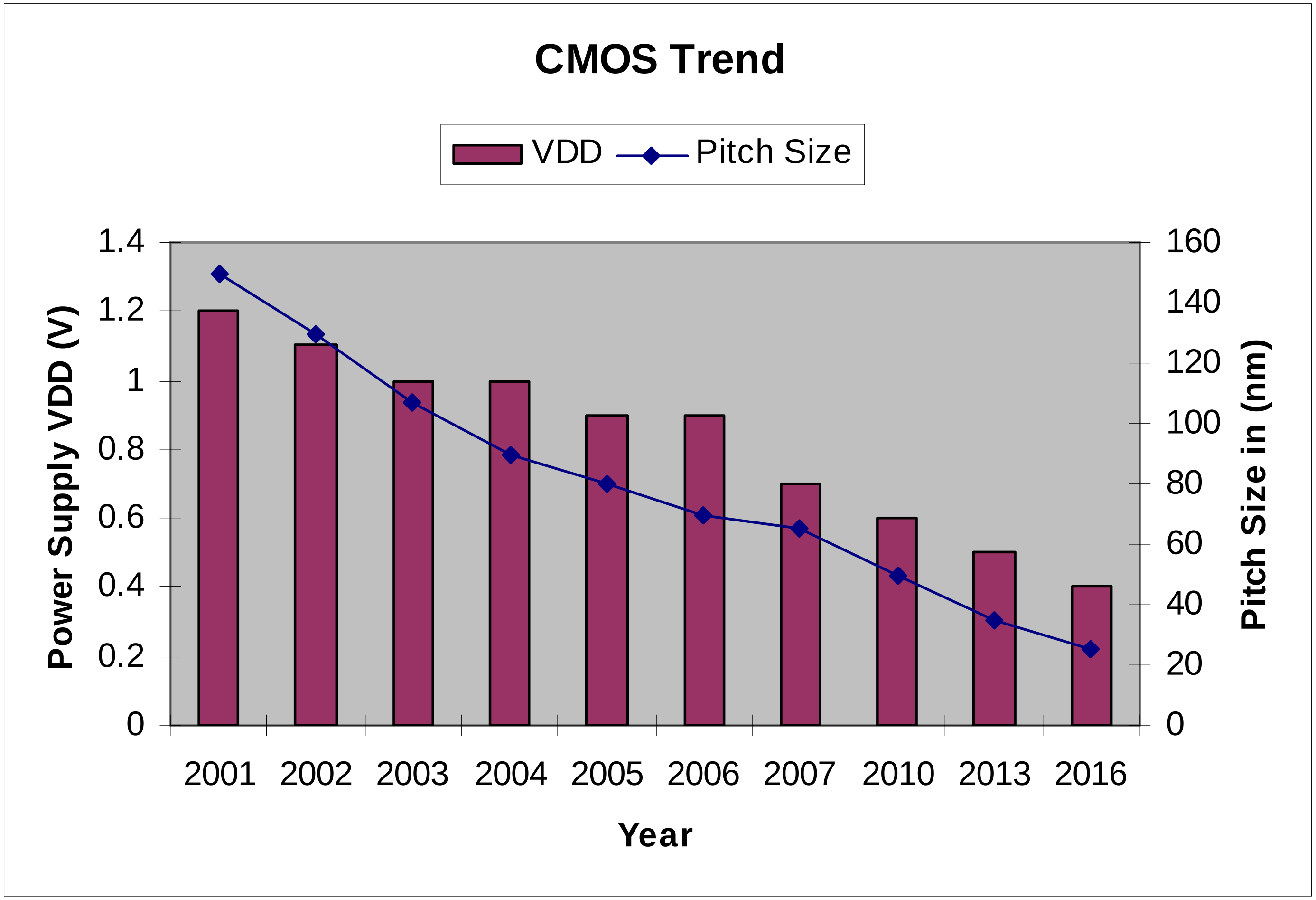
Agenda

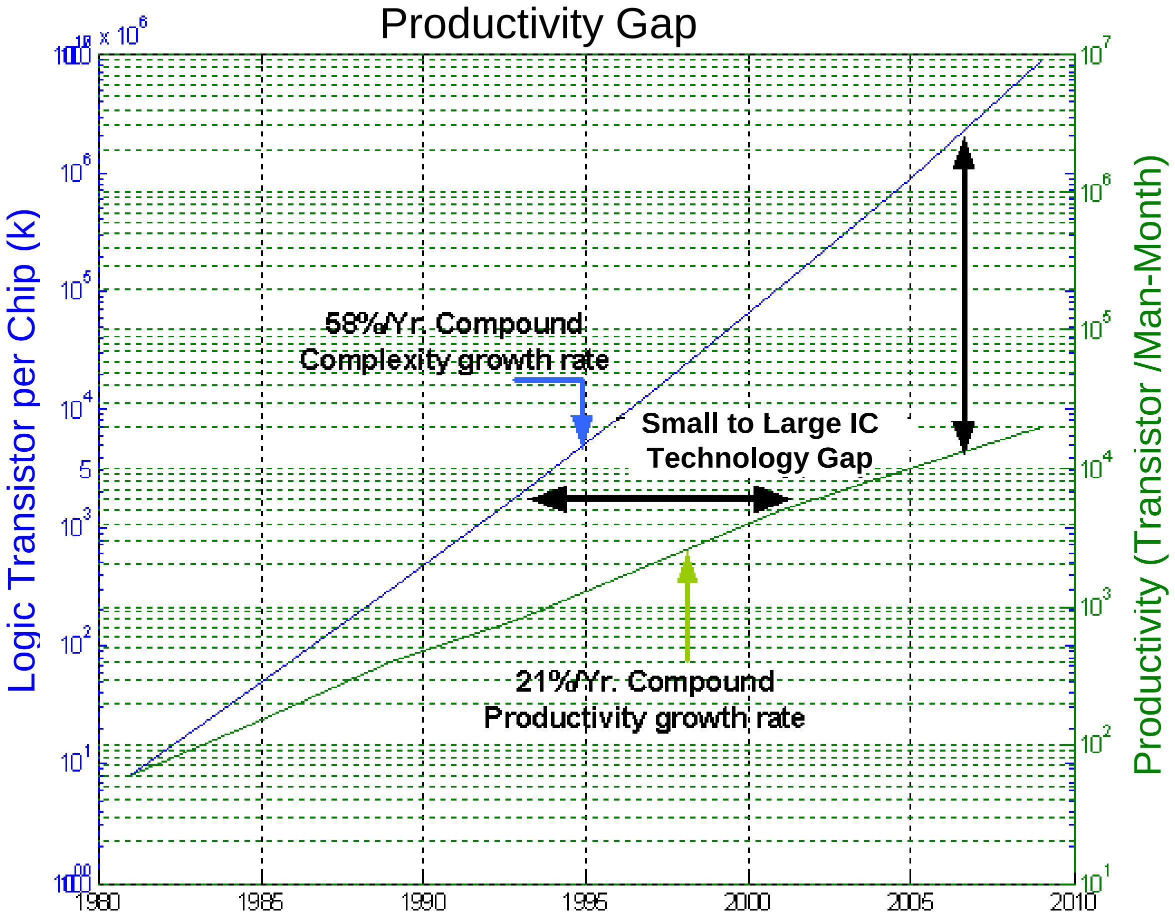
- Mainstream CMOS Mixed Signal Processes
  - *Trends in CMOS*
  - *Minimal R&D Required*
- Opportunity for Digital PWM Control
  - *Today's Analog Multiphase PWM for μP Core Regulation*
  - *Digital Communication and Monitoring*
- Benefits of Digital Control
  - *Programmability*
  - *System Reliability*
  - *Advanced Control Techniques*
- Digital Control IC Implementation
  - *Anti-Aliasing Filter*
  - *A/D Converter*
  - *Digital Pulse With Modulator*

CMOS Trends



ITRS Roadmap for High-Performance Logic Technology requirement

Leading Edge CMOS Design Productivity Gap



58%/Yr. Compound Complexity growth rate

Small to Large IC Technology Gap

21%/Yr. Compound Productivity growth rate

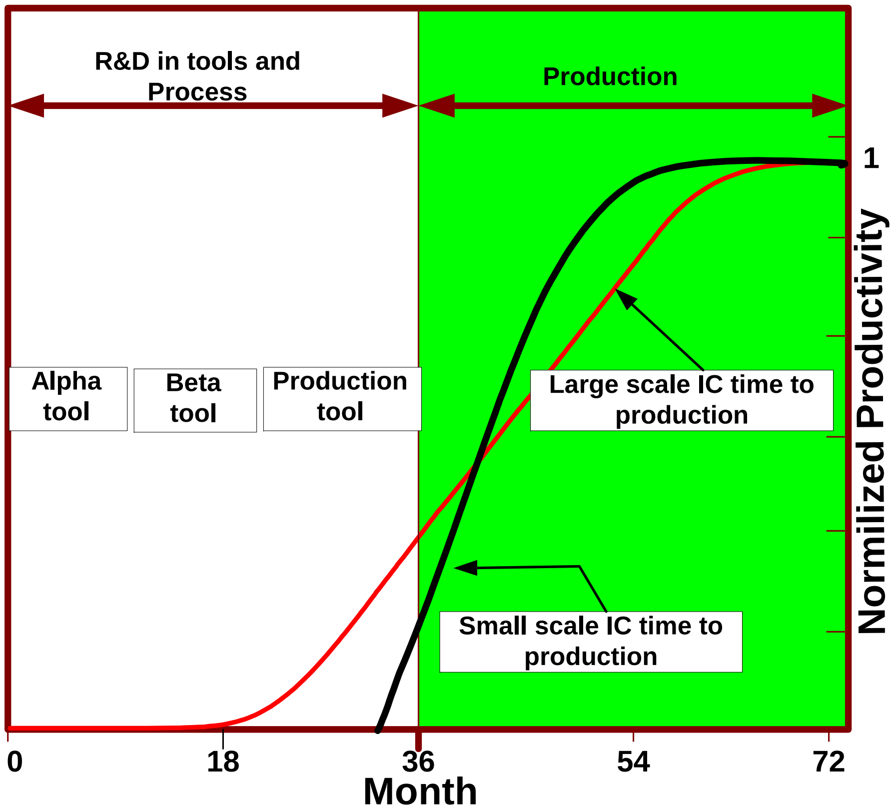
Number of Transistors per Chip Evolution

- Design Productivity not keeping pace with Moore's Law
- By Utilizing Older CMOS Technology, Designs can more Efficiently reach Production

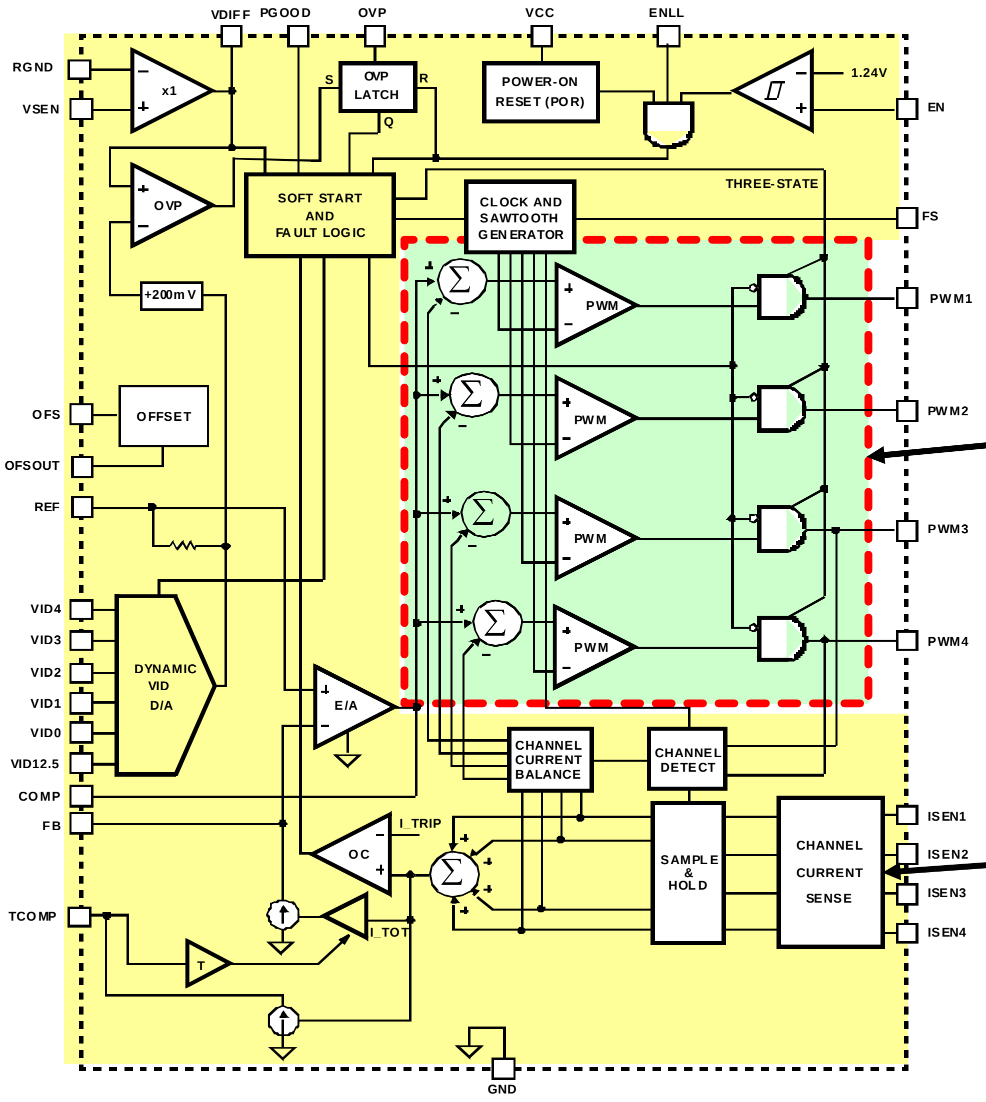
Cost Effective Approach

- Heavy R&D Investment Required for New, Leading-Edge CMOS Processes

- Designs Utilizing Older CMOS Technology
  - *Designs Cycles are Shorter*
  - *Minimal Capital Expenditures*
  - *Low Cost Relative to Leading Edge*



Analog Multiphase PWM Controllers



Today's ISL6556 Multiphase controller for Intel VR10 Applications

The only PWM required Function

System Support Functions
(VID, Ishare, Soft Start, etc.)

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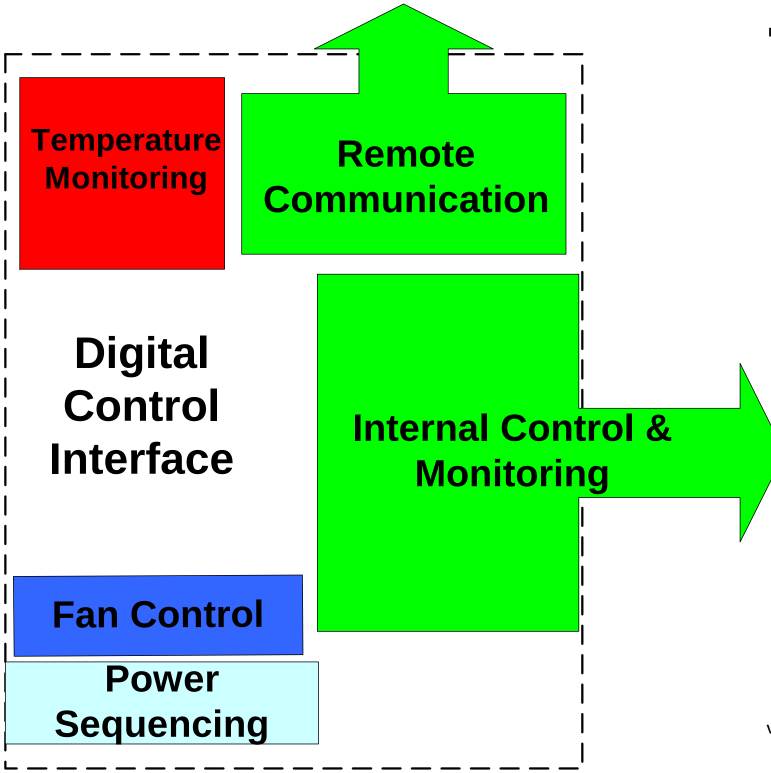
Future Multiphase Controllers



Temperature Monitoring

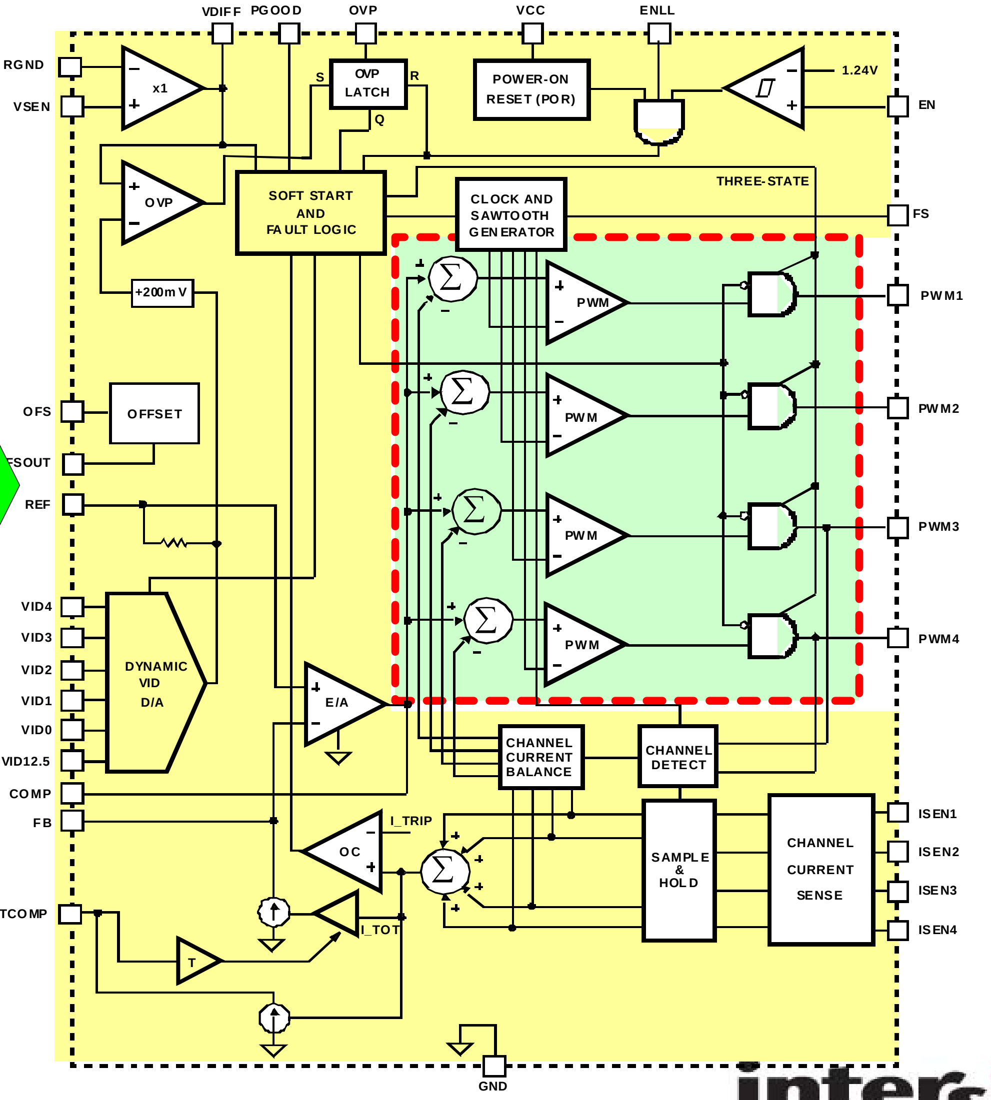
Remote Communication

Digital Control Interface

Internal Control & Monitoring

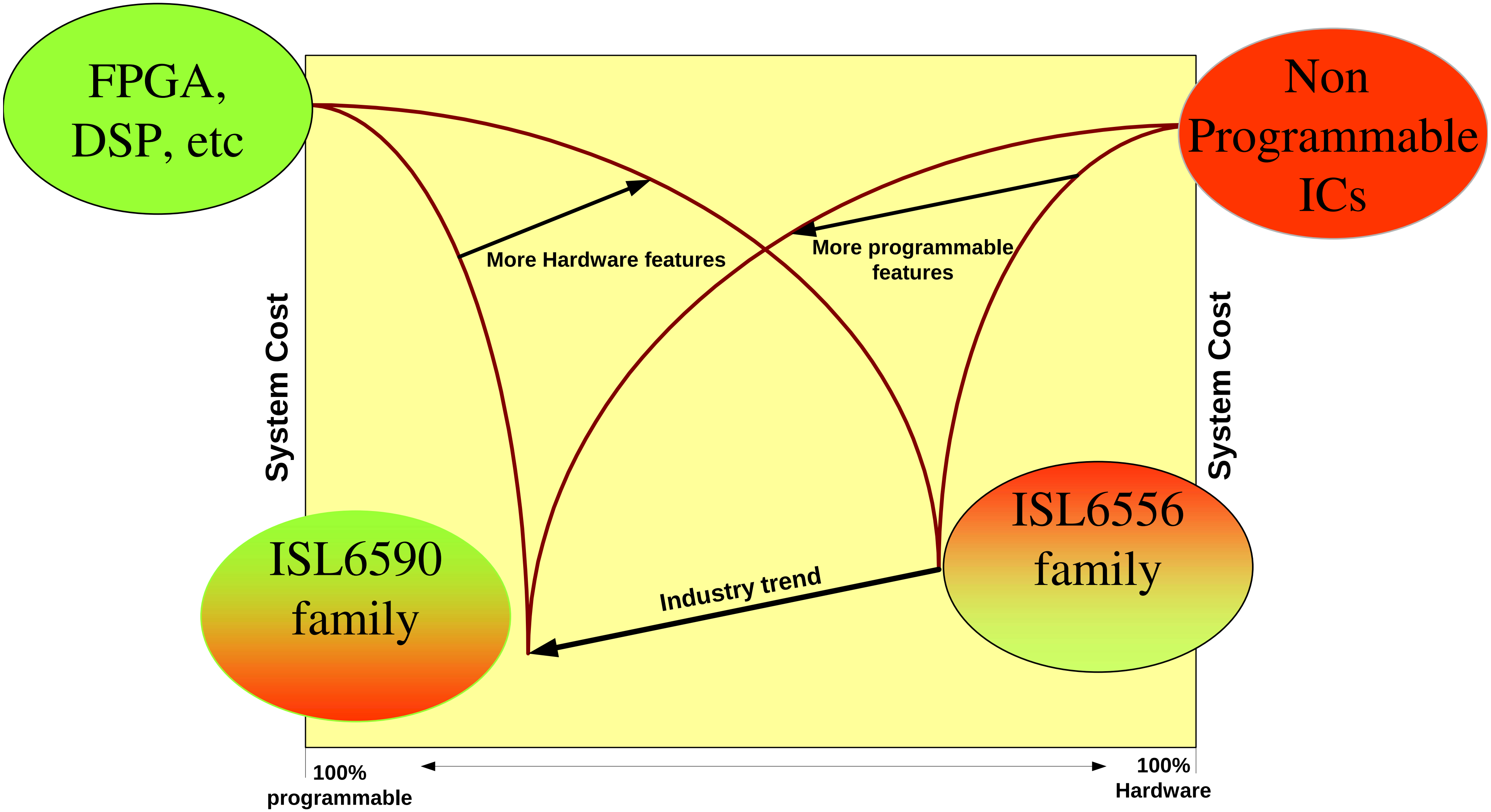
Fan Control

Power Sequencing



- Higher Integration Likely
- Digital Communication and Control can add Value

Reduced Costs via Software Programmability


FPGA, DSP, etc

Non Programmable ICs

More Hardware features

More programmable features

System Cost

System Cost

ISL6590 family

ISL6556 family

Industry trend

100% programmable

100% Hardware

Benefits of Digital Control

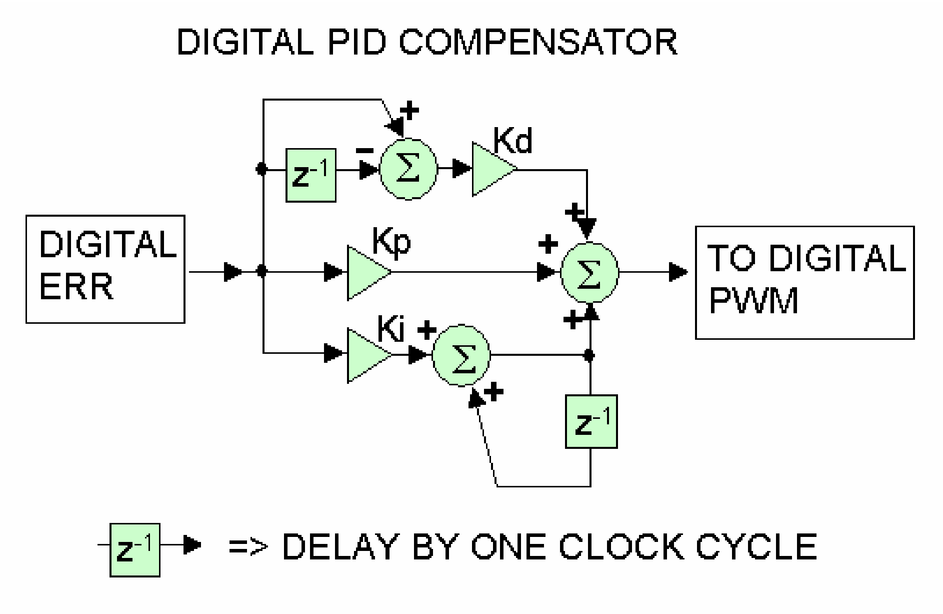
- **Programmability**
  - *Improved Flexibility / Reduced Design Time*
    - Elimination Of Discrete Component Tuning
  - *Self Calibration for Accuracy*
- **Improved System Reliability**
  - *Fewer Components*
  - *Control / Communication to Prevent Overstress*
- **Ability To Implement Advanced Control Techniques**

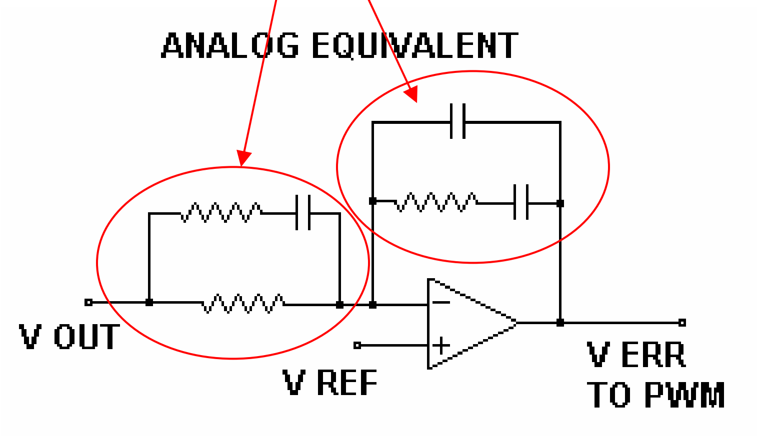
Programmability

Elimination Of Discrete Component Tuning

- **Loop Coefficient Readjustment**
  - *Compensation Filter is Digital*
  - *Frequency Response is set by Coefficients stored in Memory*

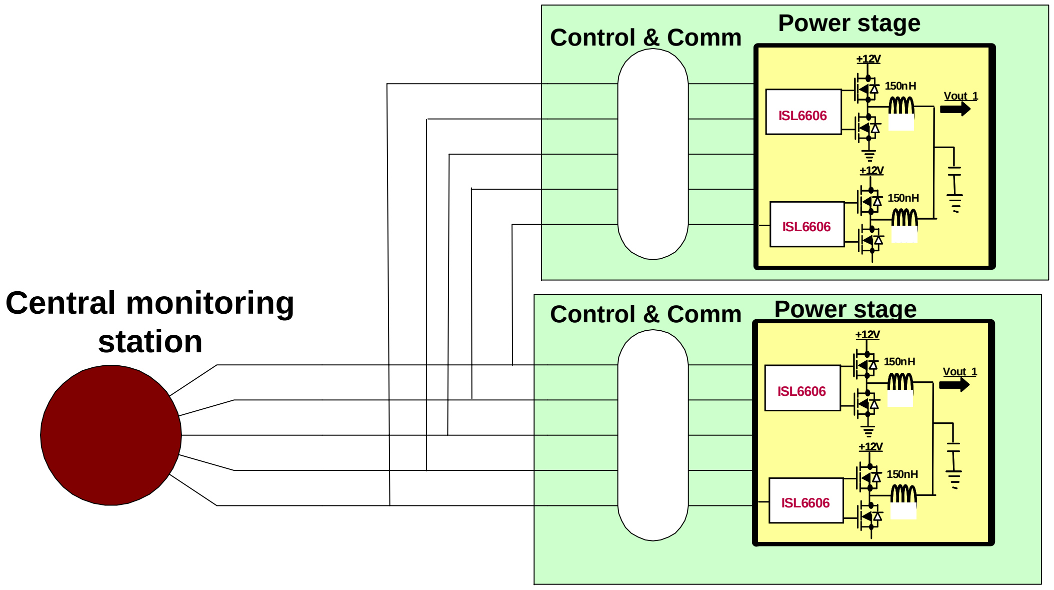
No fixed, external compensation components like Analog





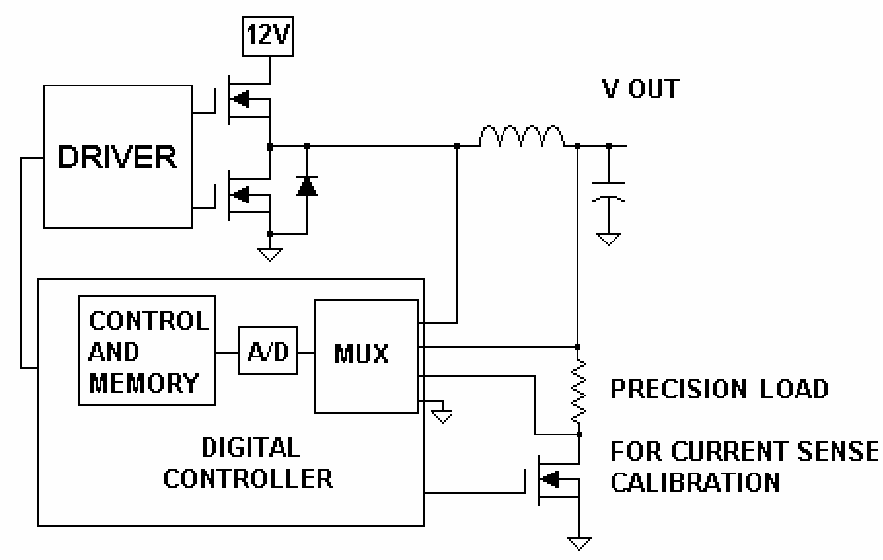
Improved Flexibility

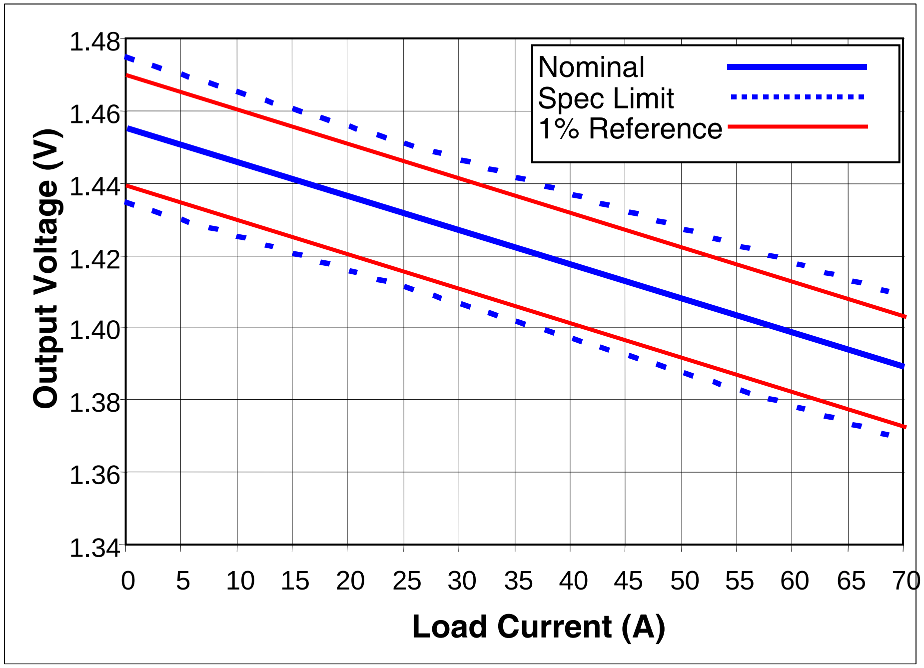
- **Eases Ability to Connect Multiple Controllers and Power Stages**
- **Easier System Integration**
  - *Communication Bus Eases Layout & Routing*



Accuracy via Calibration

- **Digital Control**
  - *Ability to Measure and Store Current Sense Calibration Data*

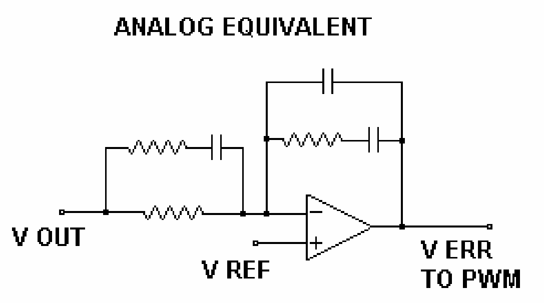




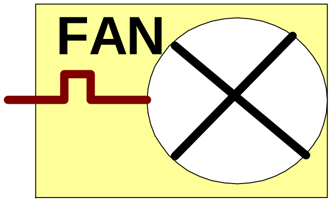
Accurate Current Sense required to meet Intel VR Loadline Specifications

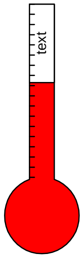
Improved System Reliability

- **Less Hardware in the System**
  - *No External IC's needed for Communication*
  - *No need for Compensation Components*



- **Protection, Prevention, and Monitoring**
  - *Fan Control to Prevent Over Temperature*
  - *Protection from Overvoltage and Overcurrent*
  - *Monitoring*
    - Temperature
    - Current, Voltage, Balancing, and Current Sharing



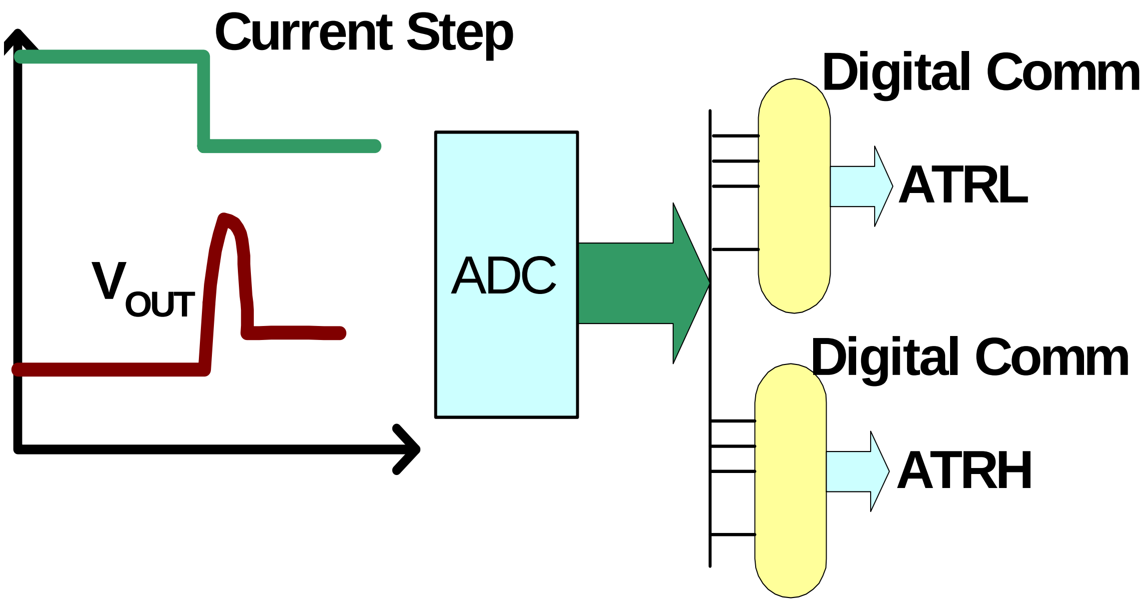


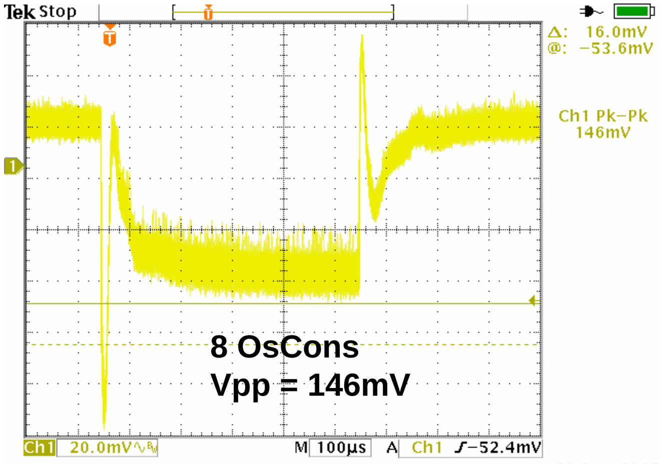
Ability To Implement Advanced Control Techniques

- Non-Linear Control
- Load Current Estimator and Predictor
- Robust Control

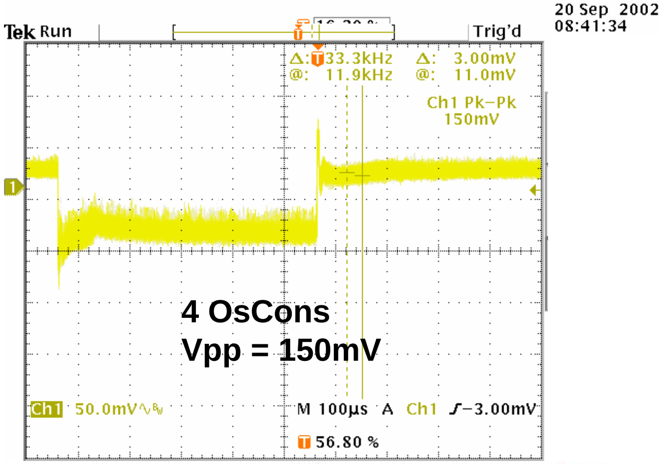
Non-Linear Control

Active Transient Response (ATR)





8 OsCons
Vpp = 146mV

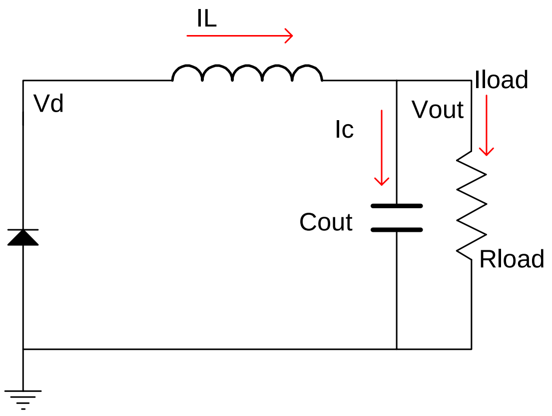


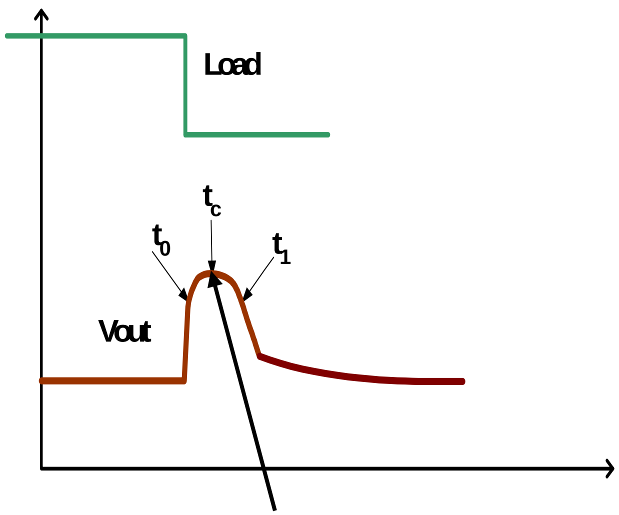
4 OsCons
Vpp = 150mV

- ➤ *ATRL turns all Lower MOSFETs OFF*
- ➤ *ATRH turns all Upper MOSFETs ON*

Load Current Estimator

<u>Equivalent Circuit when all MOSFETs are off</u>:





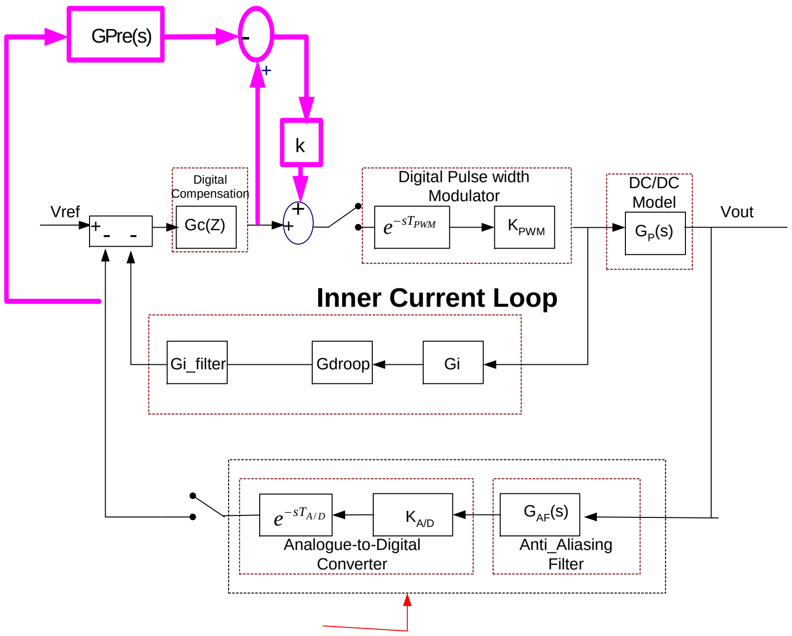
Time to measure the Inductor Current ($I_L \sim I_{LOAD}$)

- ➢ Compare Voltage Slopes
- ➢ Estimate the Current
- ➢ Simpler to Implement Timers and Counters with Digital

$$Iload(est) = IL(t_c) = \frac{(Vout + Vd)t_c}{L} + IL(t_0)$$

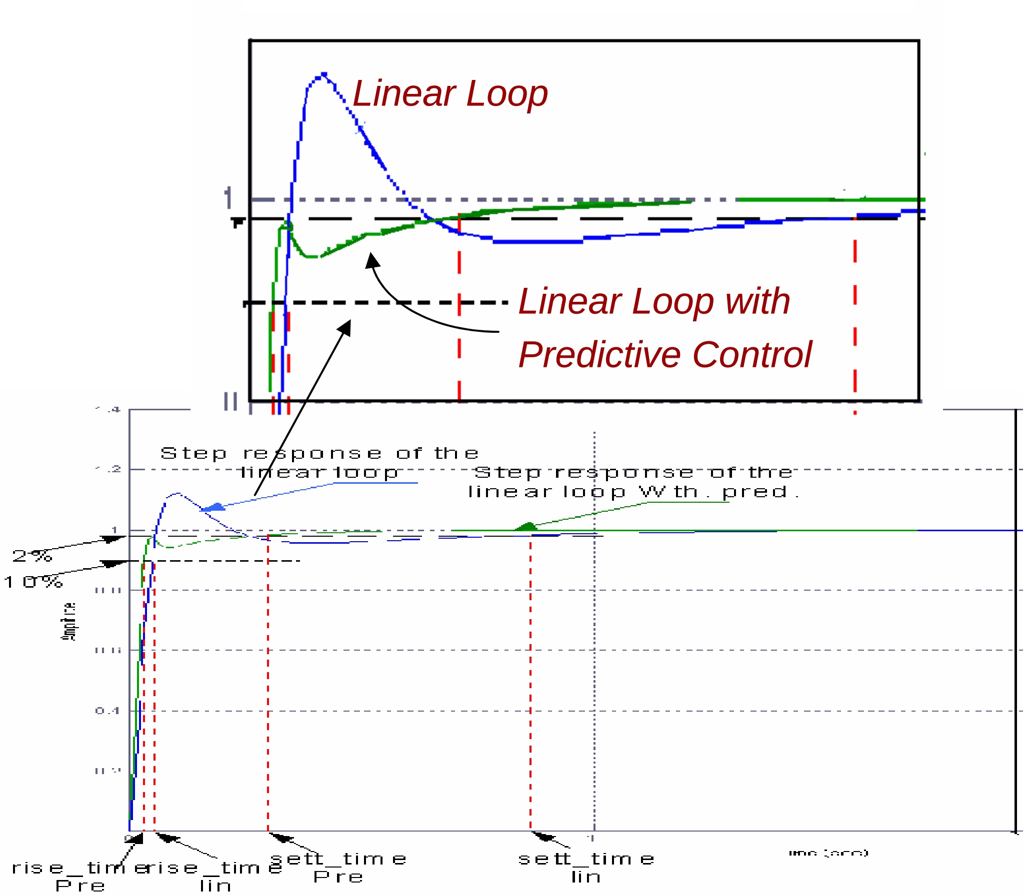
Where: Vd is the Diode Voltage
Iload(est) is the Estimated Load Current

Predictive Control



Anti_aliasing Filter + ADCM

Simulated Results



- *Rise and Settling time with Predictive Control is Reduced*
- *Predictive Control yields no Overshoot.*

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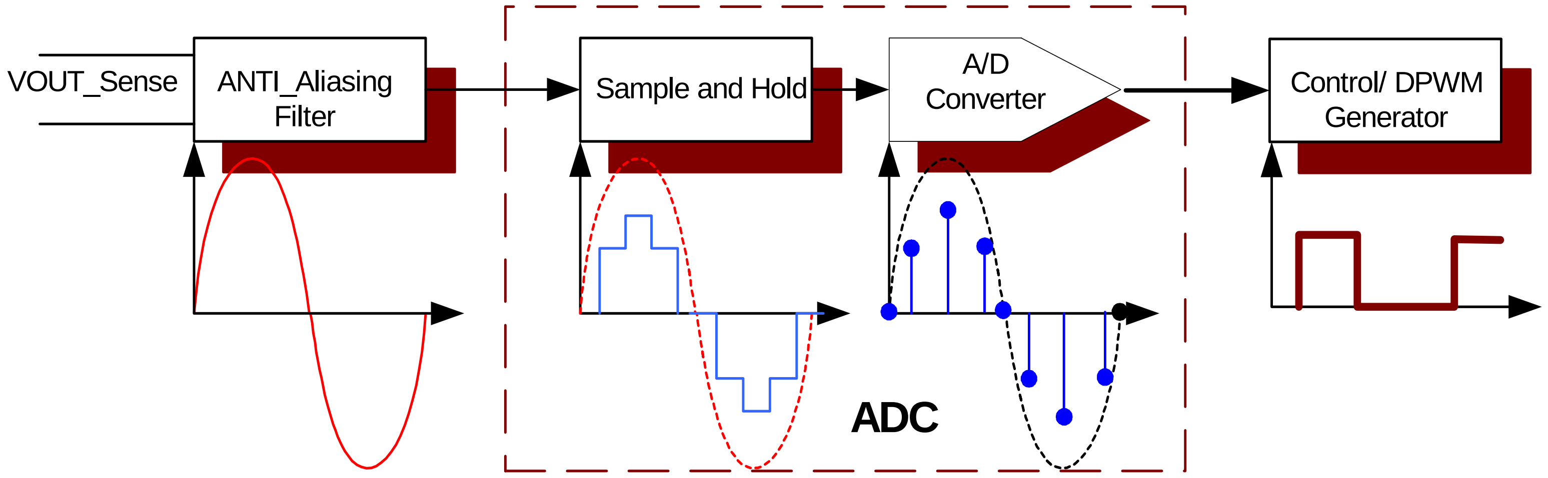
Digital Control IC Implementation

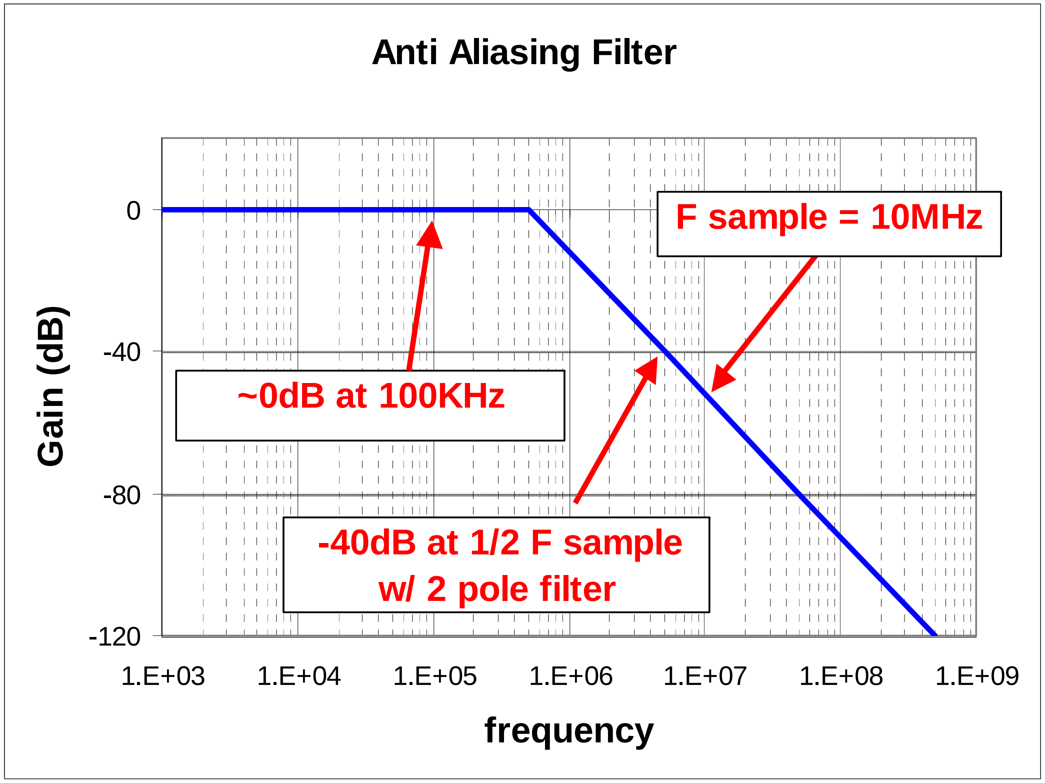
Main Digital Control Blocks

- *Anti-Aliasing Filter*
- *A/D Converter*
- *Digital PWM*



Anti-Aliasing Filter

- Anti-Aliasing Filter: Required by Sampling Theorem
- Unity DC Gain and Minimum Phase Lag before Main Loop Cutoff requires:
  - *High Sampling Frequency*
  - *High order filter (2nd order or higher)*



Analog to Digital Converter

- ***Sample and Hold Front End***
  - Introduces a delay = $e^{-sT_{ADC}}$
- ***ADC Architectures***

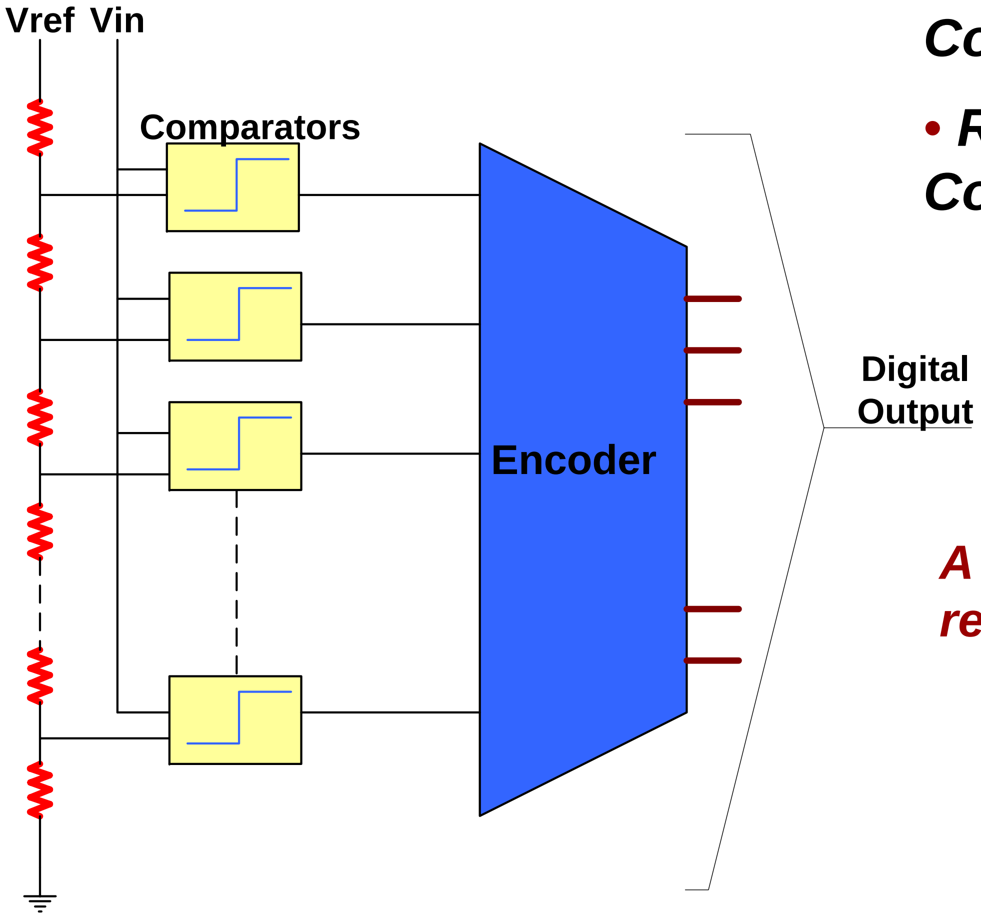
  (1) **Flash** - set of $2^n - 1$ comparators used

  (2) **Successive Approximation** - uses a single comparator, introduces nT_{ADC} delay

  (3) **Pipelined with Multiple Flash** – uses p consecutive stages with n-bit D/A

ADC Architectures
Flash

Flash uses a set of 2^n-1comparators for an n-bit ADC



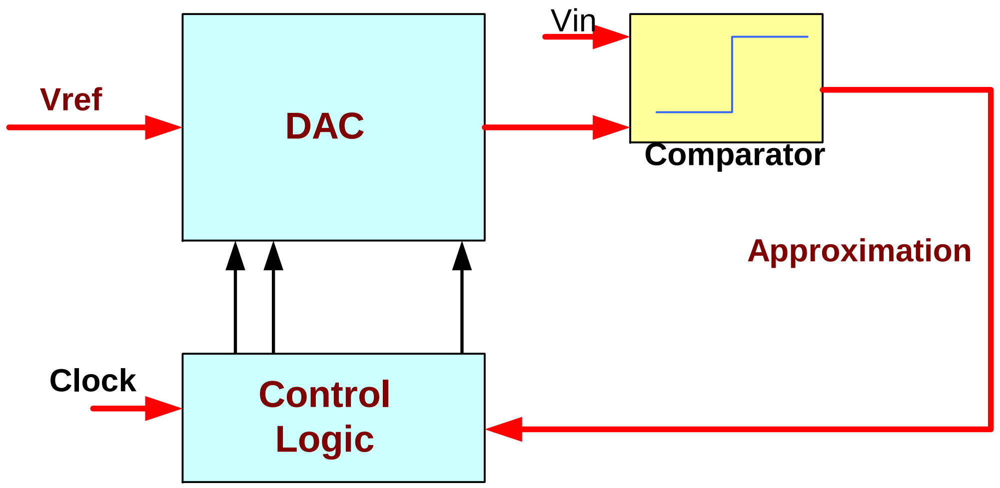
- ***Very Fast - only one Cycle to Convert***
- ***Requires Large Number of Comparators***

A 10-bit Converter would require 1023 Comparators!

ADC Architectures

Successive Approximation

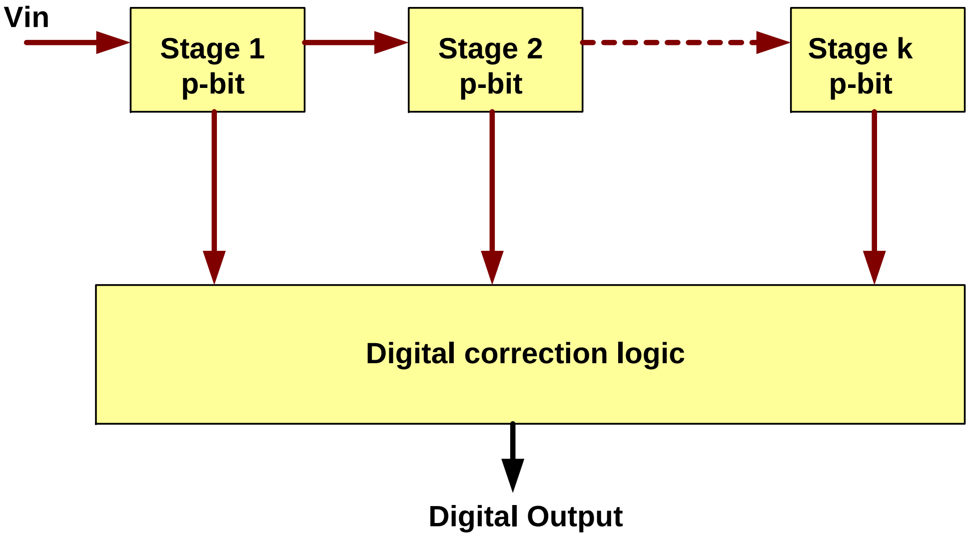
Successive Approximation Register (SAR)



- Simple, Low Gate Count
  - *Requires only a Single Comparator to realize a High Resolution ADC*
- Slow
  - *Requires n Comparisons for an n-bit Resolution*
  - *Delay =* nT_{ADC}

ADC Architectures
Pipelined with Multiple Flash

Pipelined with Multiple Flash



- ***Requires p SAR stages and k=n/p Flash A/D for an n-bit ADC***
- ***Slower than Flash; faster than SAR (Delay = kT_{ADC})***
- ***Requires far more Comparators than SAR --> $k(2^P-1)$***

Summary of ADC Architectures

ADC Comparison	10-bit Flash	10-bit SAR	10-bit 2-stage Pipeline
#Comparators	1023	1	62
Delay	T_{ADC}	$10T_{ADC}$	$2T_{ADC}$

ADC Architectures
Number of Bits Required

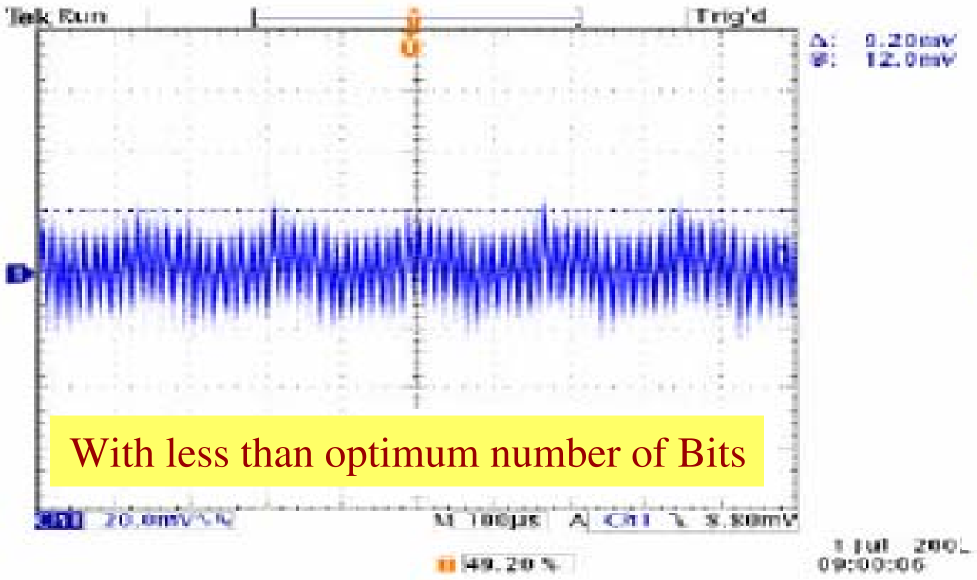
$$\Delta V_{out} G \geq \frac{V_{ADC\max}}{2^{n_{adc}}} \qquad n_{adc} = \mathrm{int}(\log_2(\frac{V_{ADC\max}}{\Delta V_{out} G}))$$

Where:

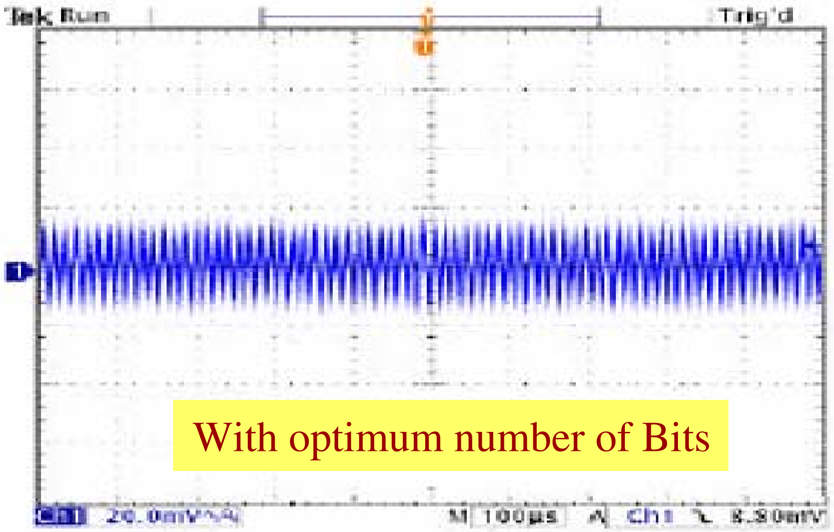
G = the voltage scaling

ΔV_{out} = the output voltage requirement

n_{adc} = the minimum ADC number of bits



With less than optimum number of Bits



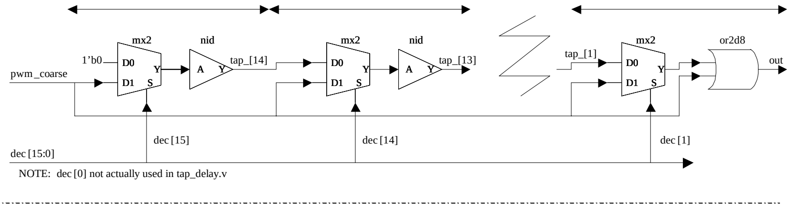
With optimum number of Bits

Digital PWM

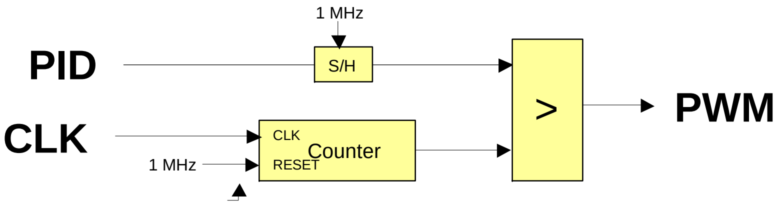
- ✓ ***Digital PMW produces a Discrete and Finite PWM width***
- ✓ ***Minimum Number of Bits needed depends on the Topology***

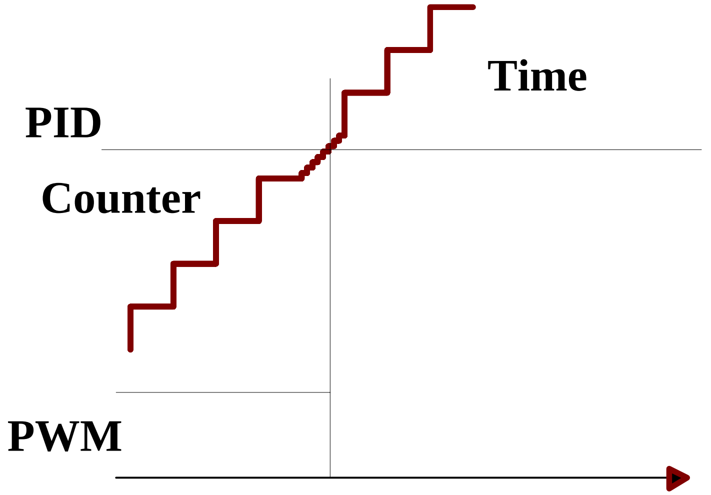
For Buck Converter :

$$V_{out} = DV_{in}$$



pwm_gen.v





k_{pwm} = the DPWM minimum number of bits

$$k_{pwm} = \text{int}(n_{adc} + \log_2(\frac{GV_{out}}{V_{ADC\max}D}))$$

n_{adc} = the ADC number of Bits

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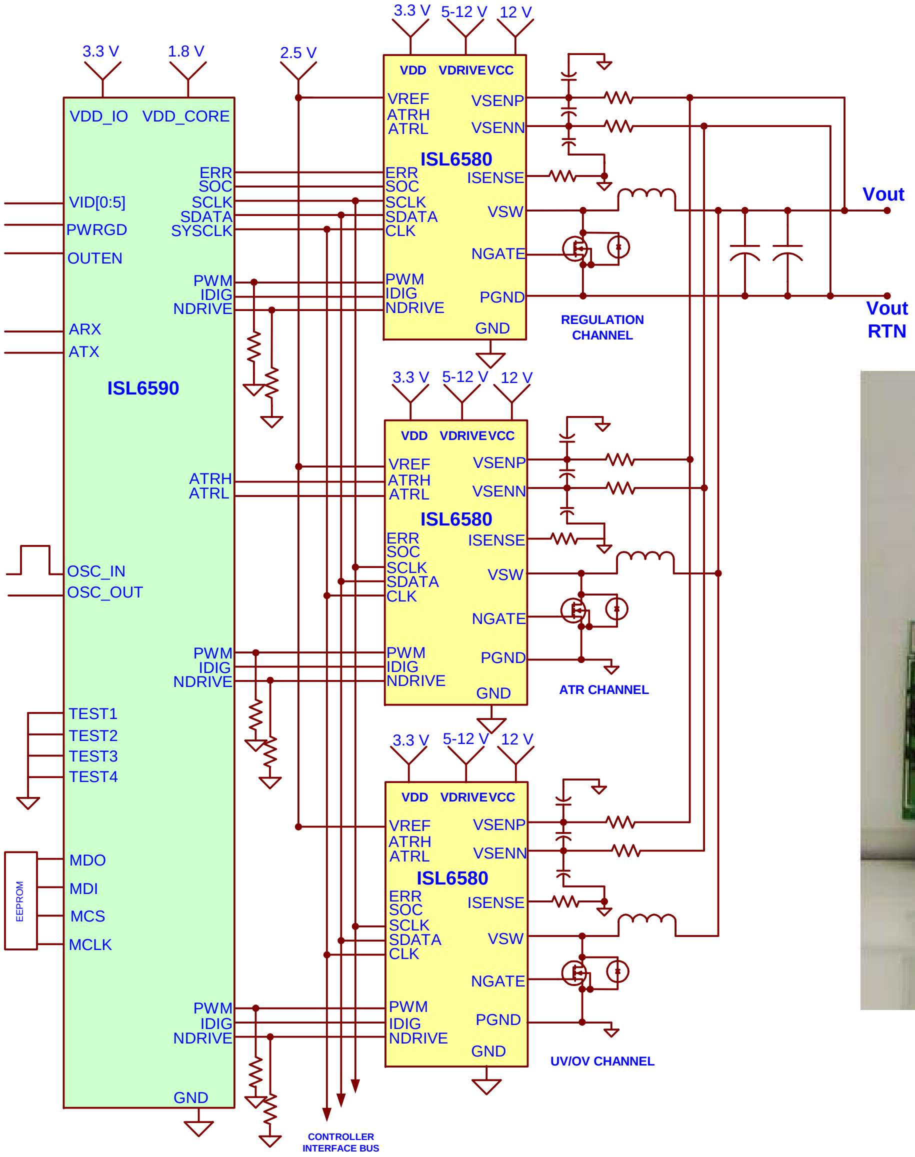
Complete Digitally Controlled Power System



ISL6590/80 forms a Complete Digital Multiphase Solution

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Conclusion

- Opportunity for Digital PWM Control
  - *Cost Effective*
  - *Digital Communication and Monitoring*
  - *Programmability*
  - *System Reliability*
  - *Advanced Control Techniques*
- Digital Control IC Implementation
  - *Anti-Aliasing Filter*
  - *A/D Converter*
  - *Digital Pulse With Modulator*