



Advancements in Power Semiconductor Solutions

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The Goal: An Ideal Power Switch

Zero Power Loss:

Zero voltage drop when device is conducting current ie. "on-state"

Zero current flowing when device is blocking voltage ie. "off-state"

Zero losses to switch between the "on-state" and "off-state"

Small Footprint

Zero Cost

Power Losses

$$\Delta T = R_{th} \left\{ (V_{on} \times I_{on}) + \left(\int V(t) \times I(t) dt \right) f \right\}$$

Thermal
Component

On-State
Component

Switching
Component

Voltage Regulator Module Synchronous Buck Converter

Low Side MOSFET

Minimize $R_{ds(on)}$

Low Q_g

Shoot through immunity

Low diode losses

High Side MOSFET:

Low Figure of Merit: $R_{ds(on)} \times Q_{gd}$

Low Voltage MOSFET Evolution

Planar Power MOSFET



Trench Power MOSFET

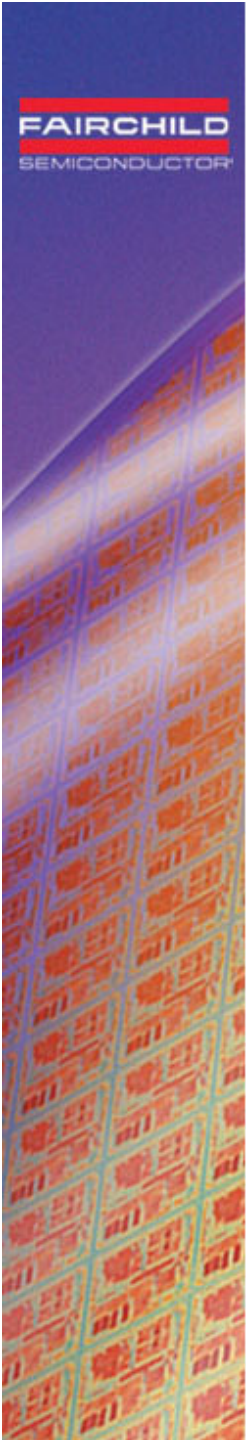


Advanced Structures:

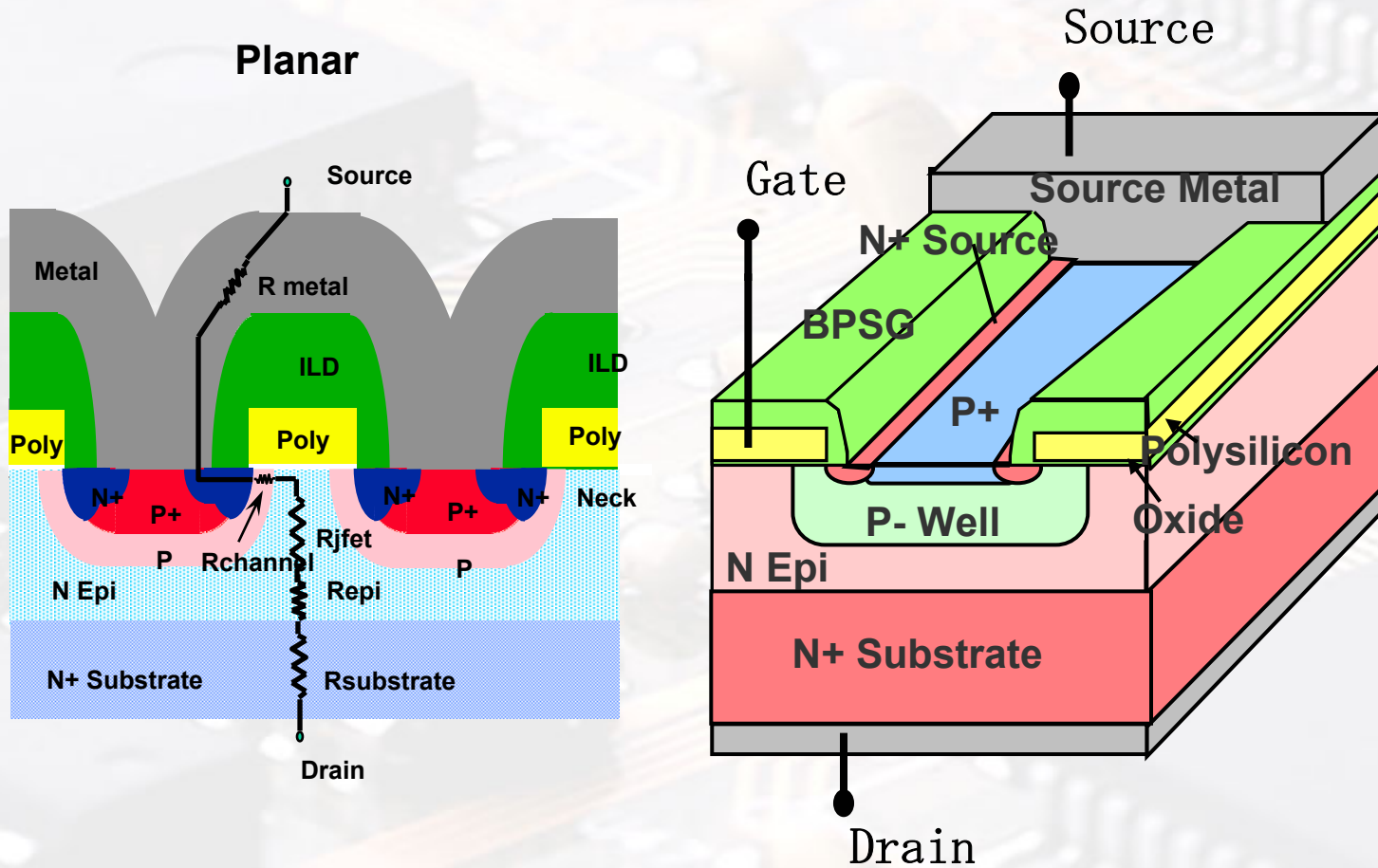
Low Q_g



Charge Balance
Lateral MOSFET

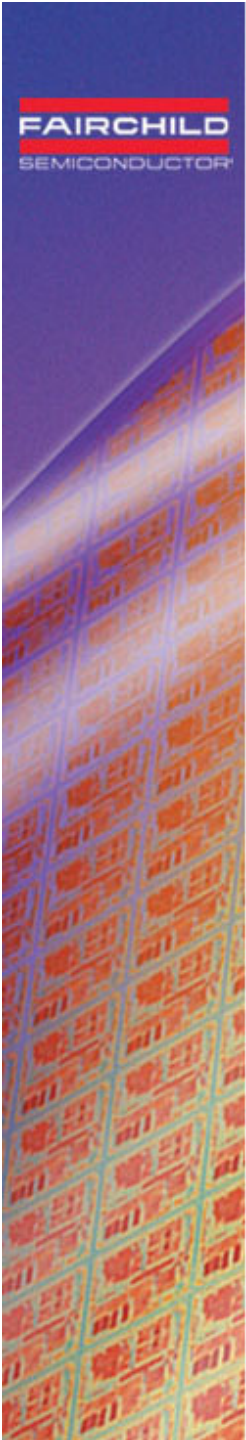


Planar Power MOSFET

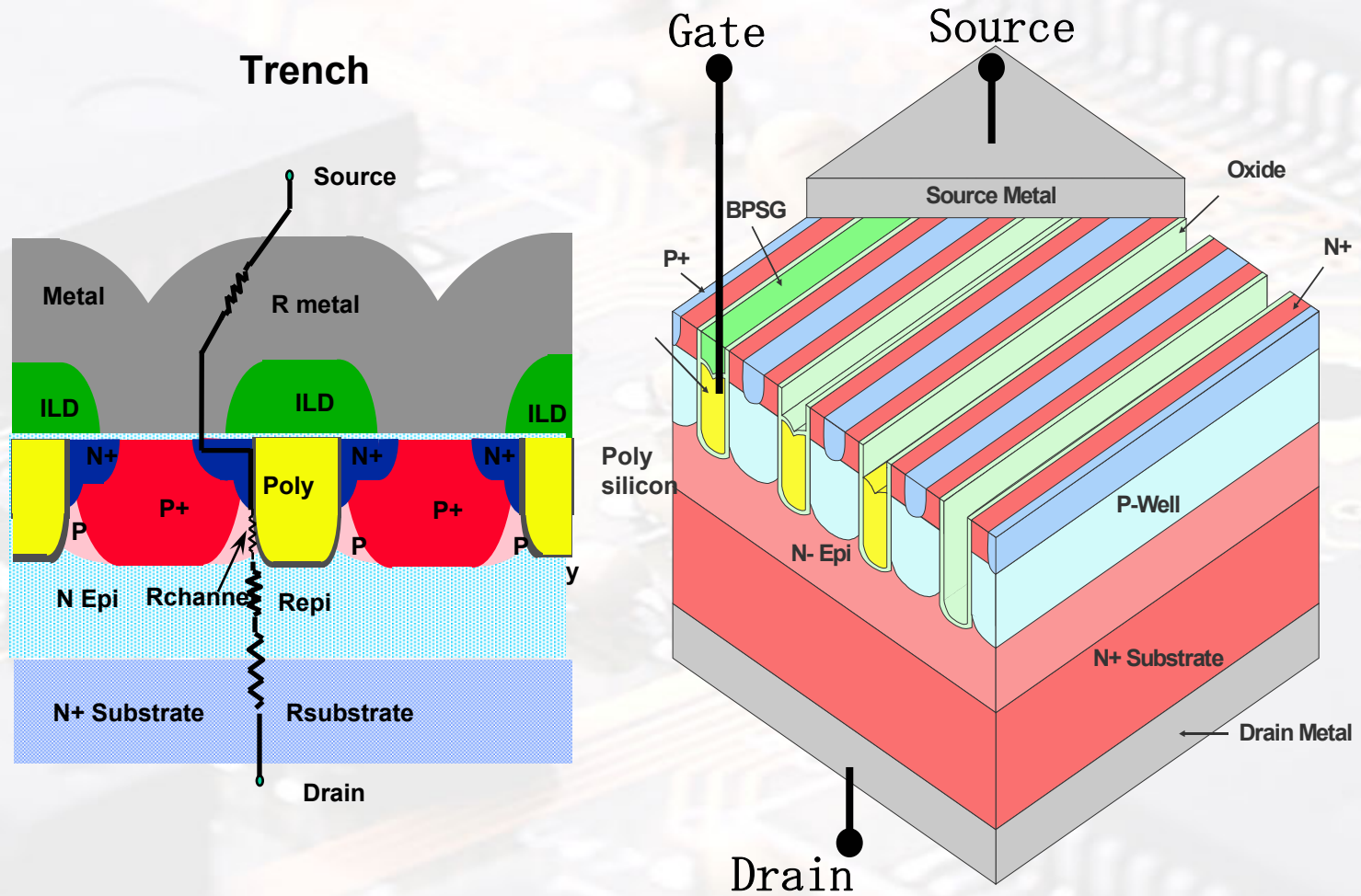


$$R_{ds(on)} = R_{sub} + R_{epi} + R_{jfet} + R_{channel} + R_{source} + R_{metal}$$

R_{jfet} and R_{epi} components limit scaling



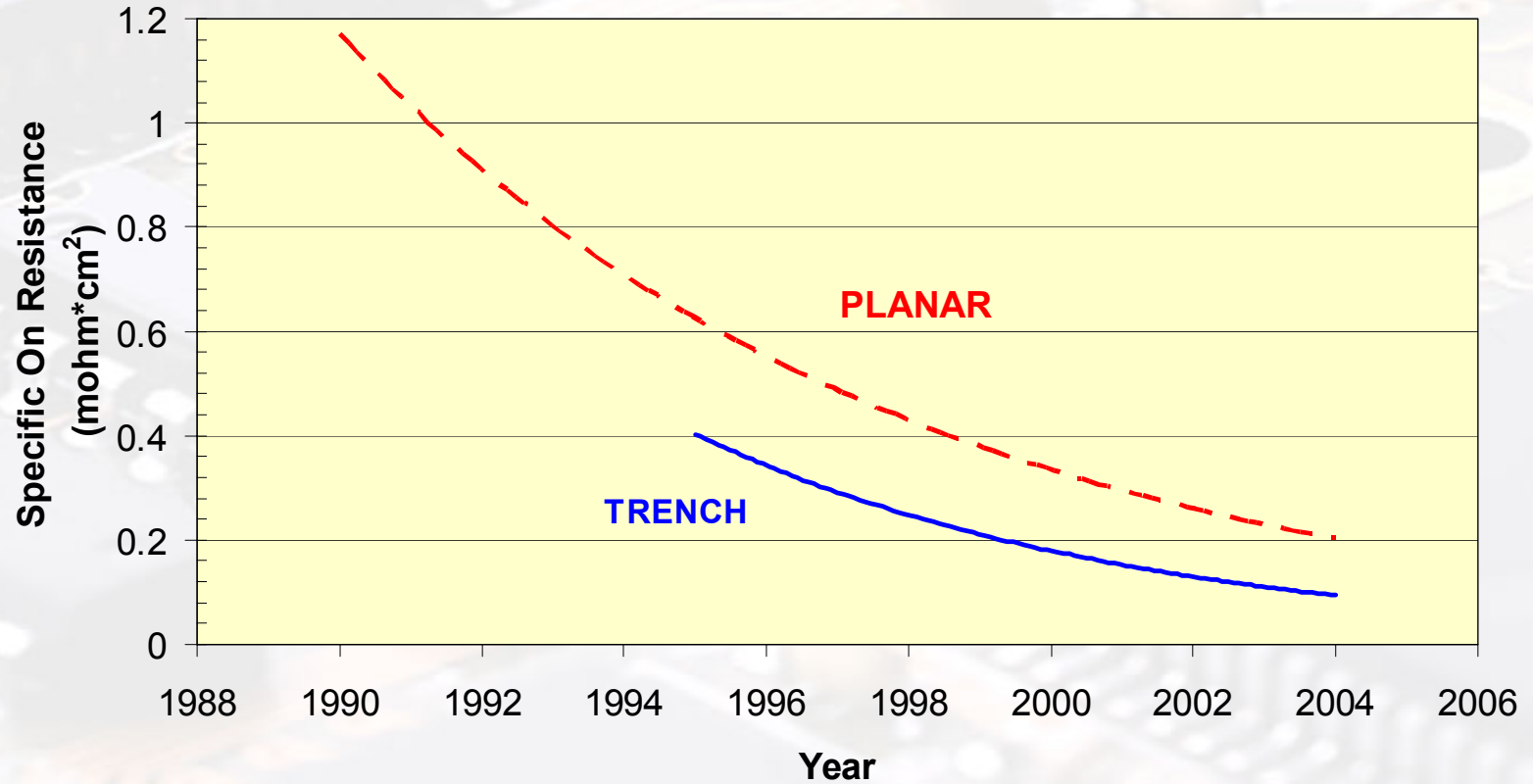
Trench Power MOSFET



$R_{ds(on)} = R_{sub} + R_{epi} + R_{channel} + R_{source} + R_{metal}$
 Elimination of R_{jfet} permits device scaling

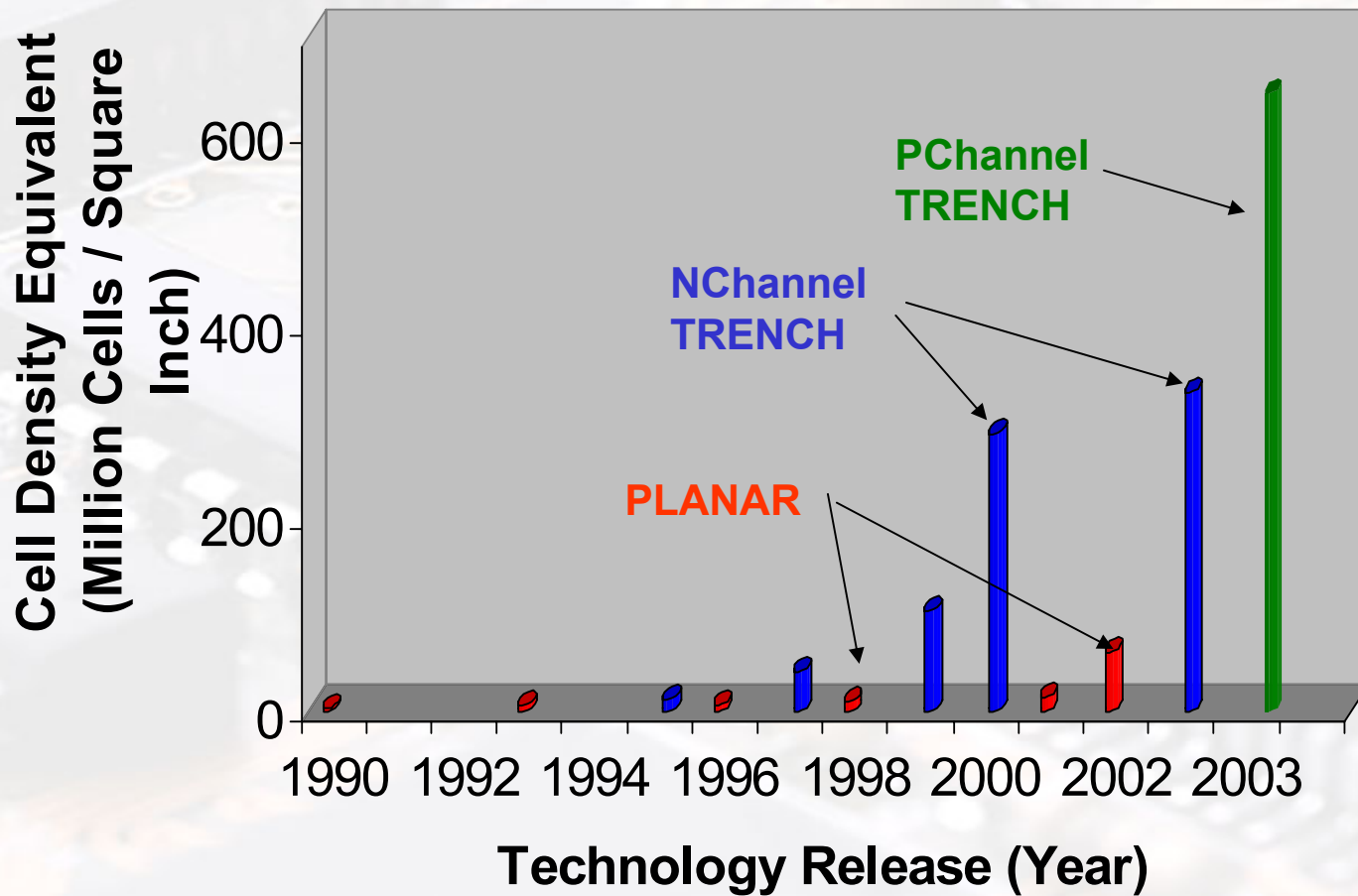
Industry Low Voltage MOSFET Resistance Trend

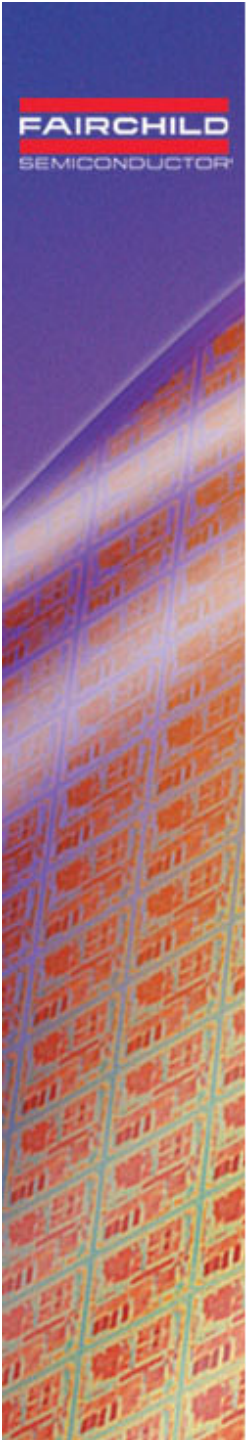
**R_{ds(on)} Performance
30V N-Channel Product**



Industry Cell Density Progression

Cell Density Trend



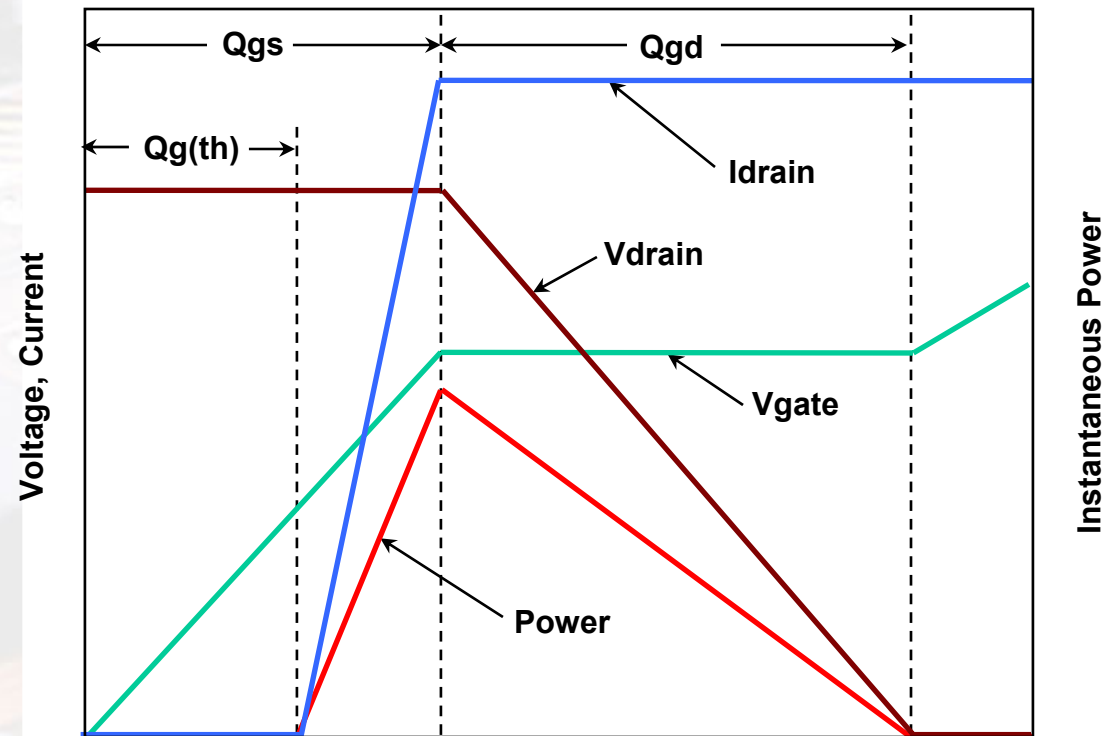


DC/DC Converter MOSFET Characteristics

**Hard Switching
Losses**

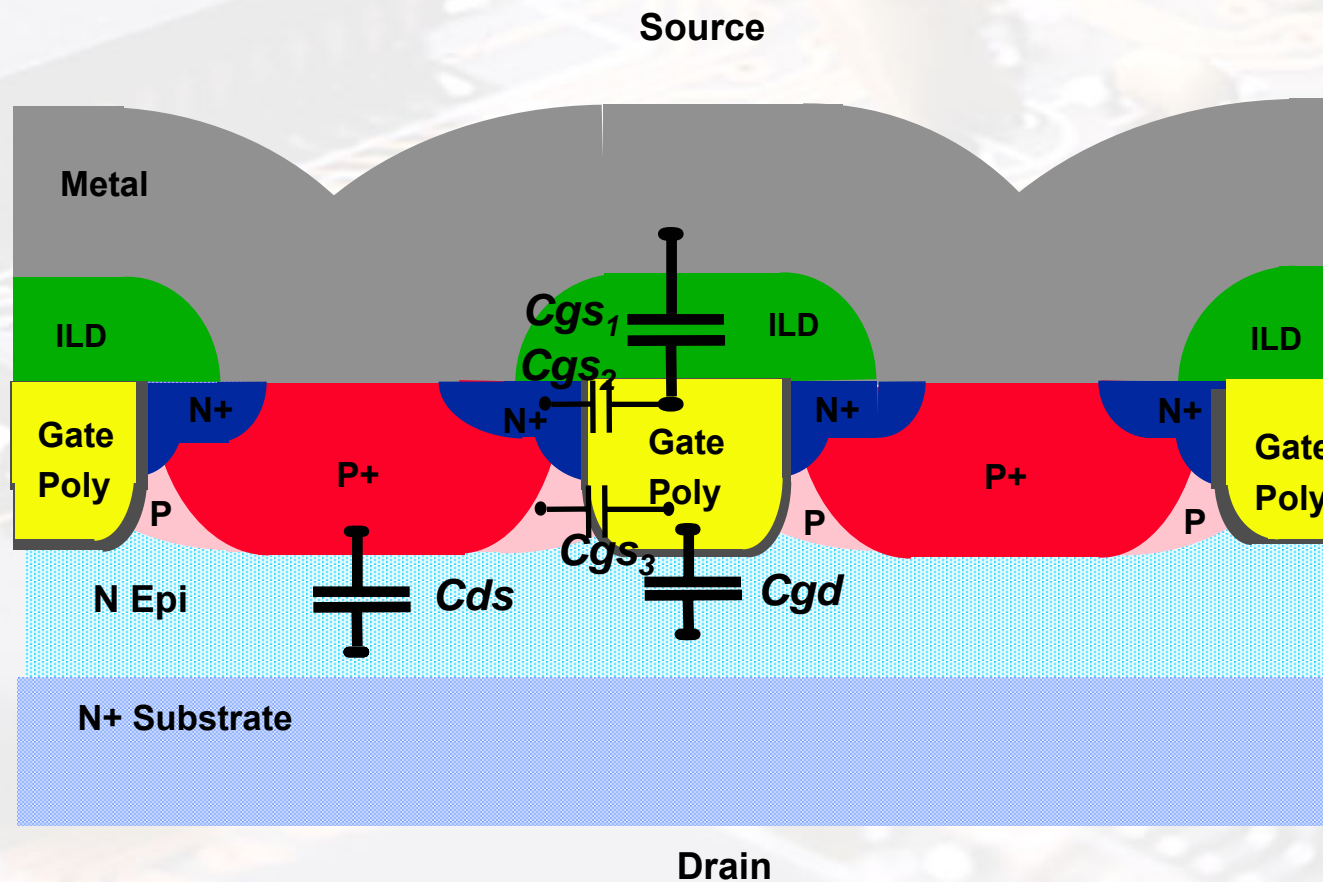
**Power Dissipated
During Turn-On
and Turn-Off**

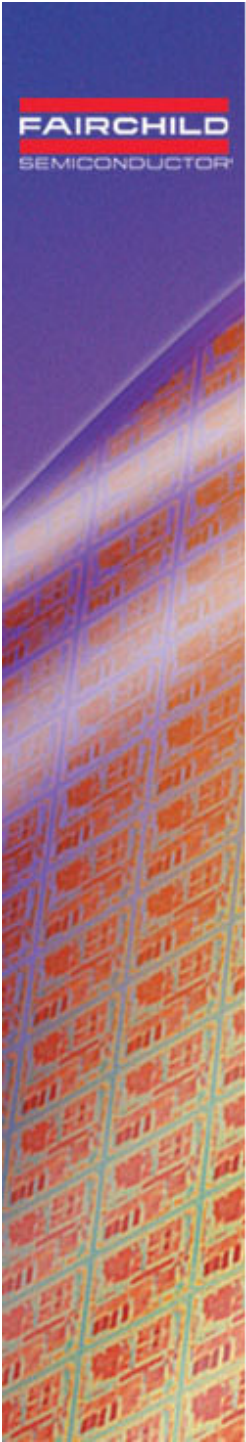
Ideal Switching Waveforms



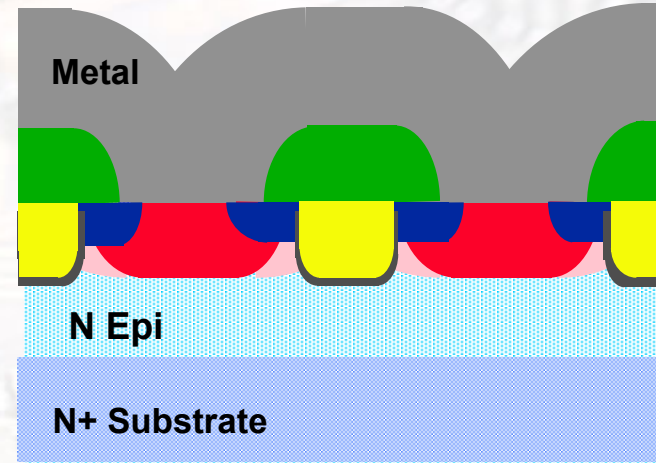
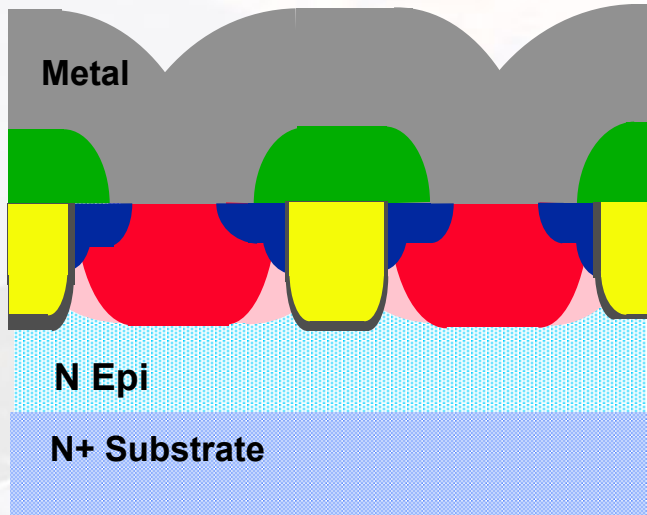
Need to Reduce Q_g to Reduce Switching Losses

Capacitances Impacting Gate Charge

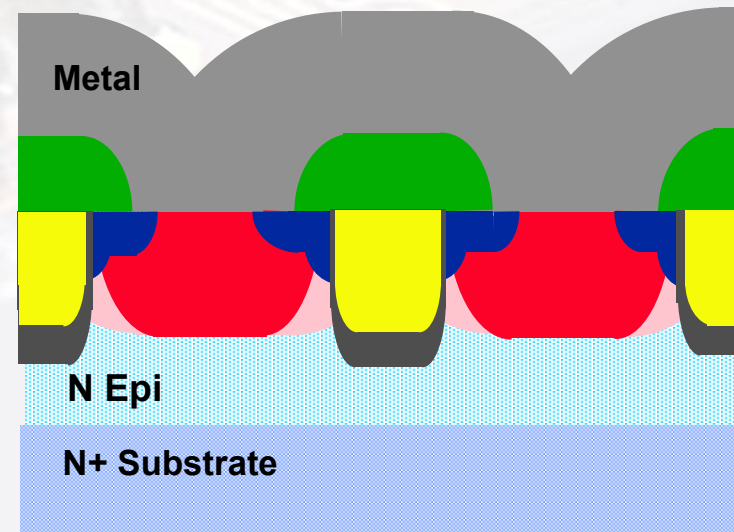
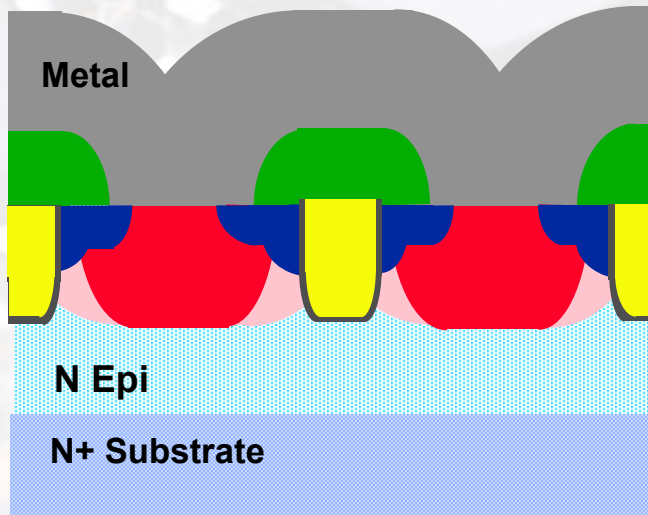


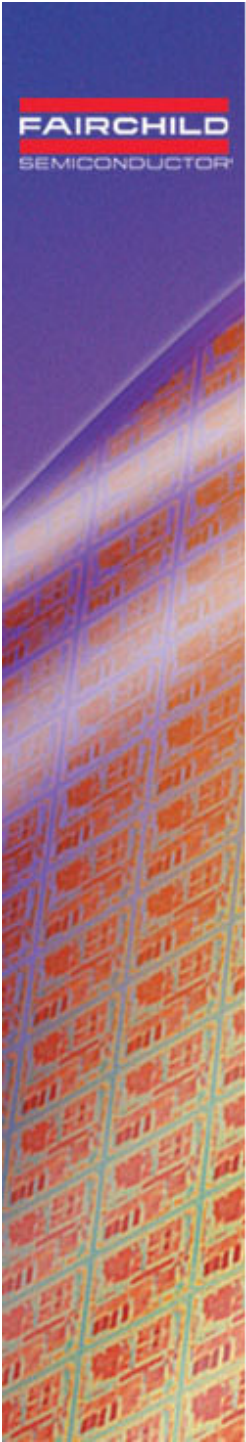


Gate Charge Reduction

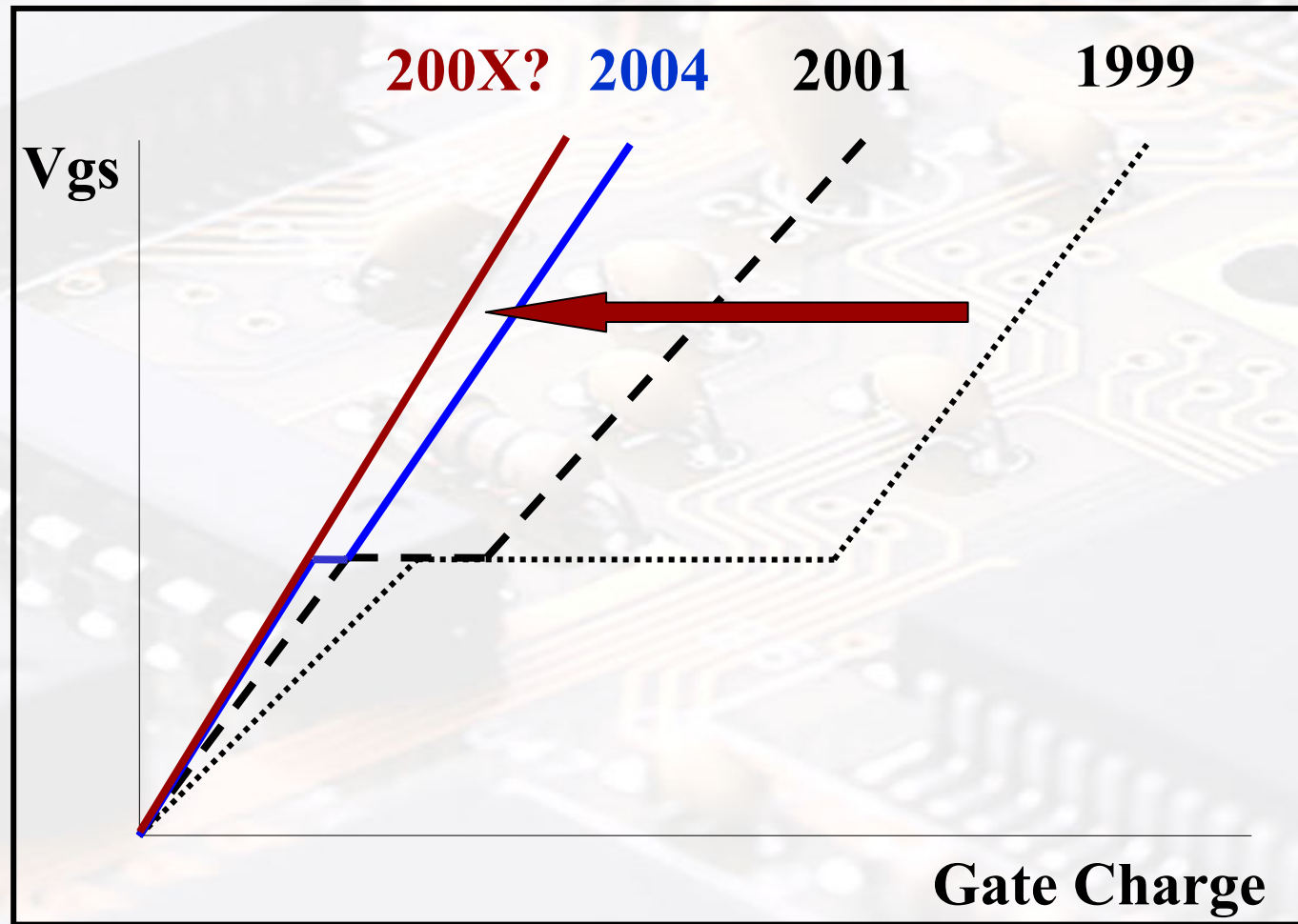


$$C = \frac{\epsilon * \text{Area}}{\text{Thickness}}$$





Gate Charge Reduction Trend



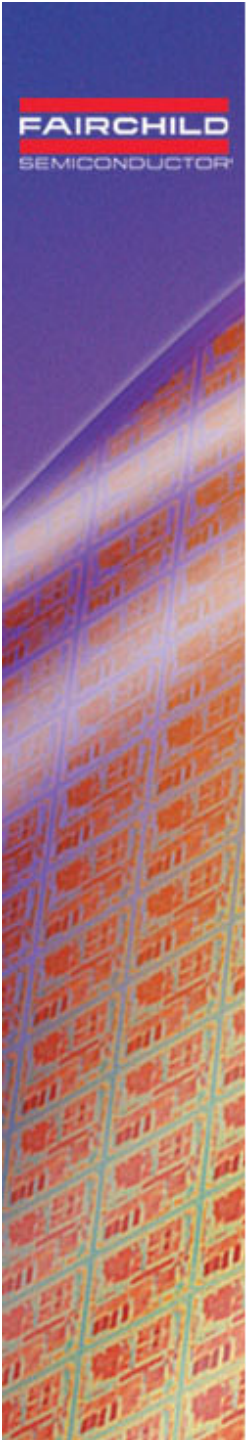
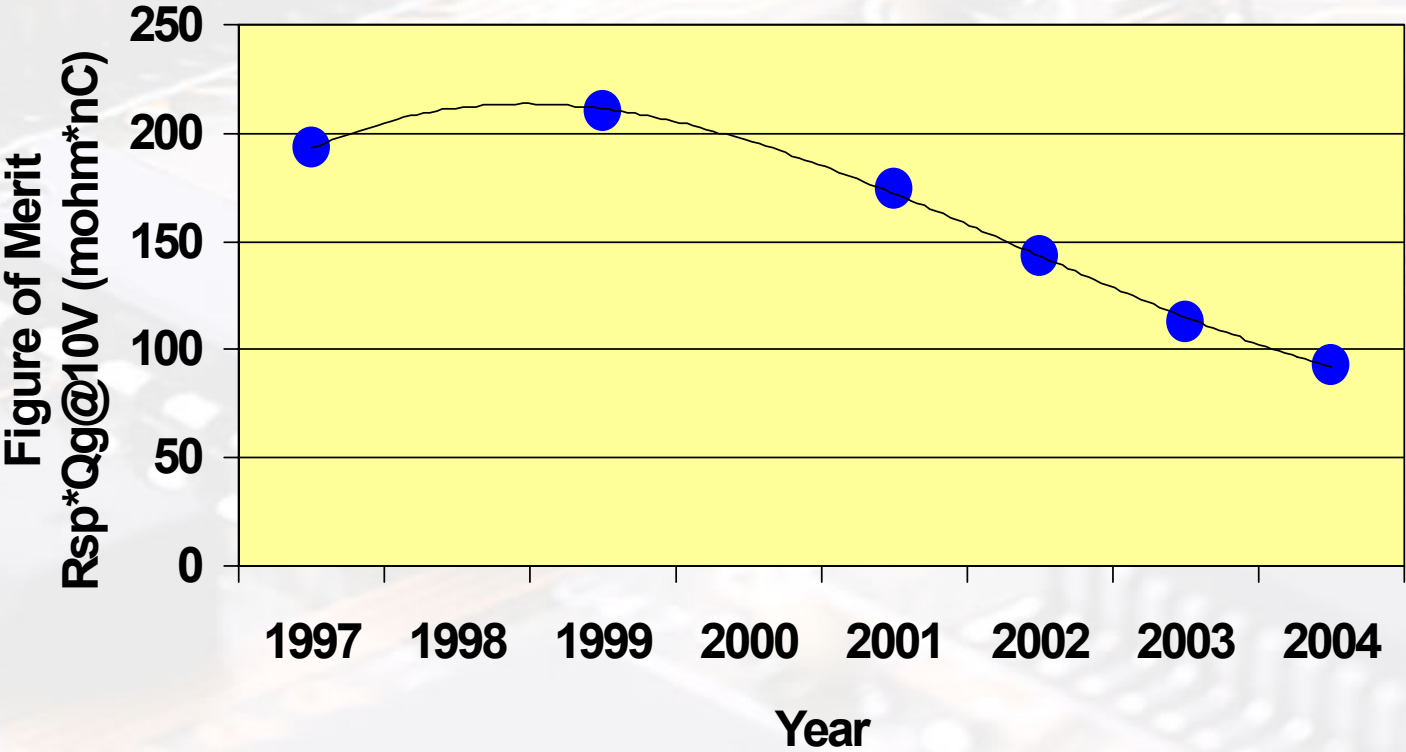


Figure of Merit Trend

$R_{on} * Q_g(10)$

Figure of Merit vs. Time



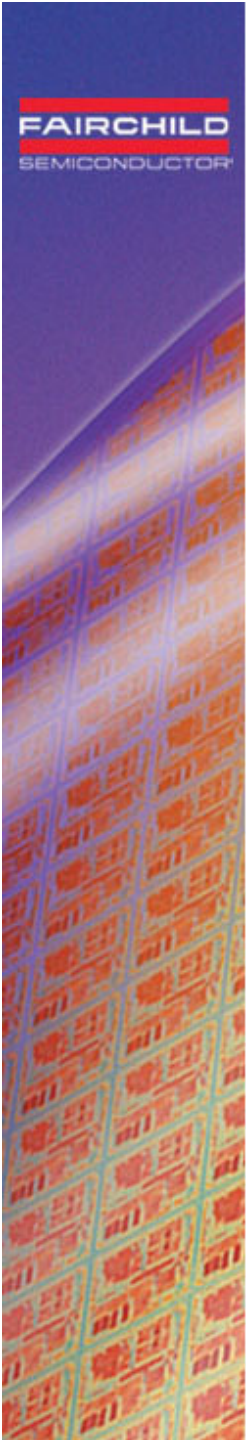
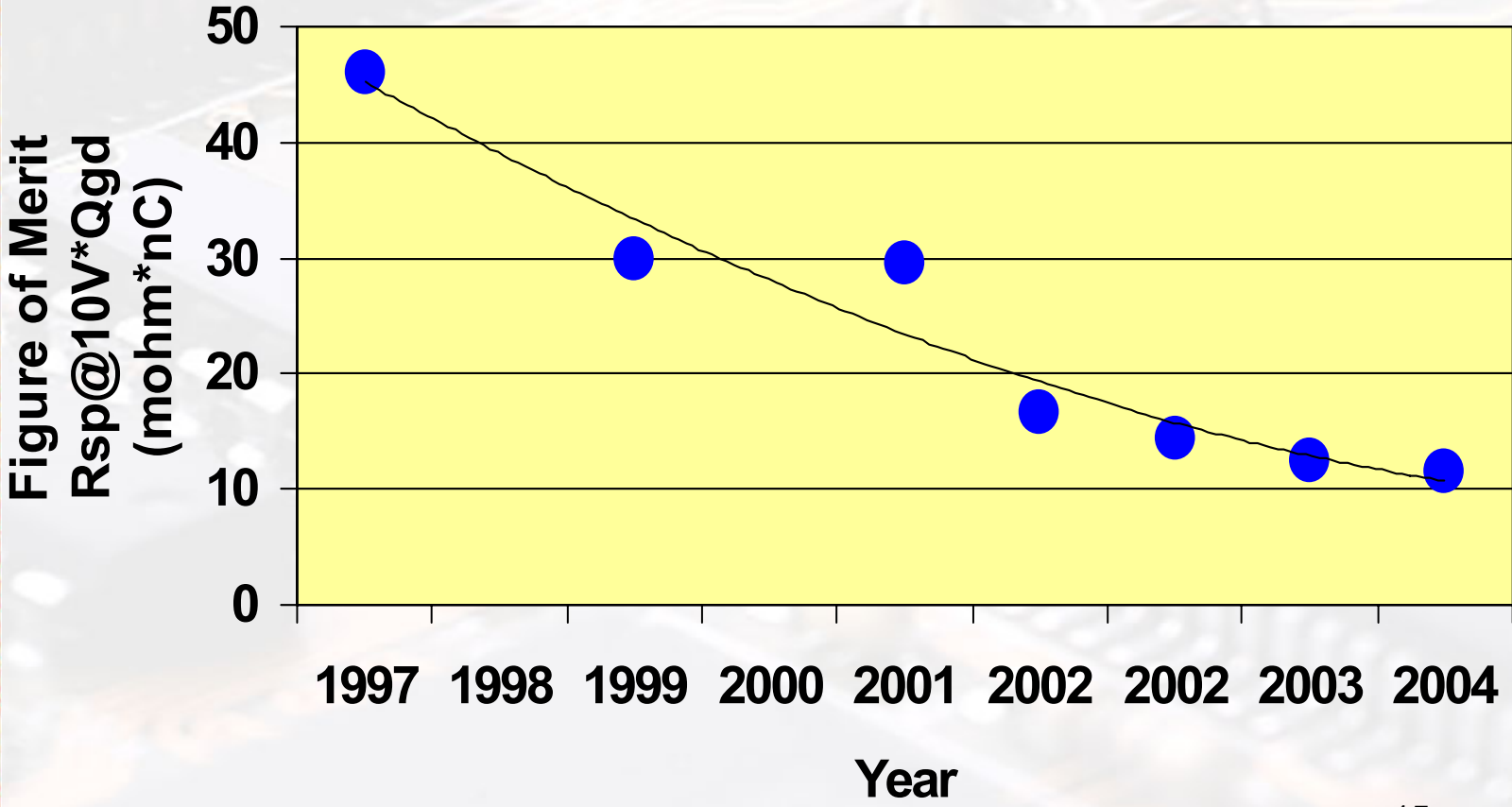


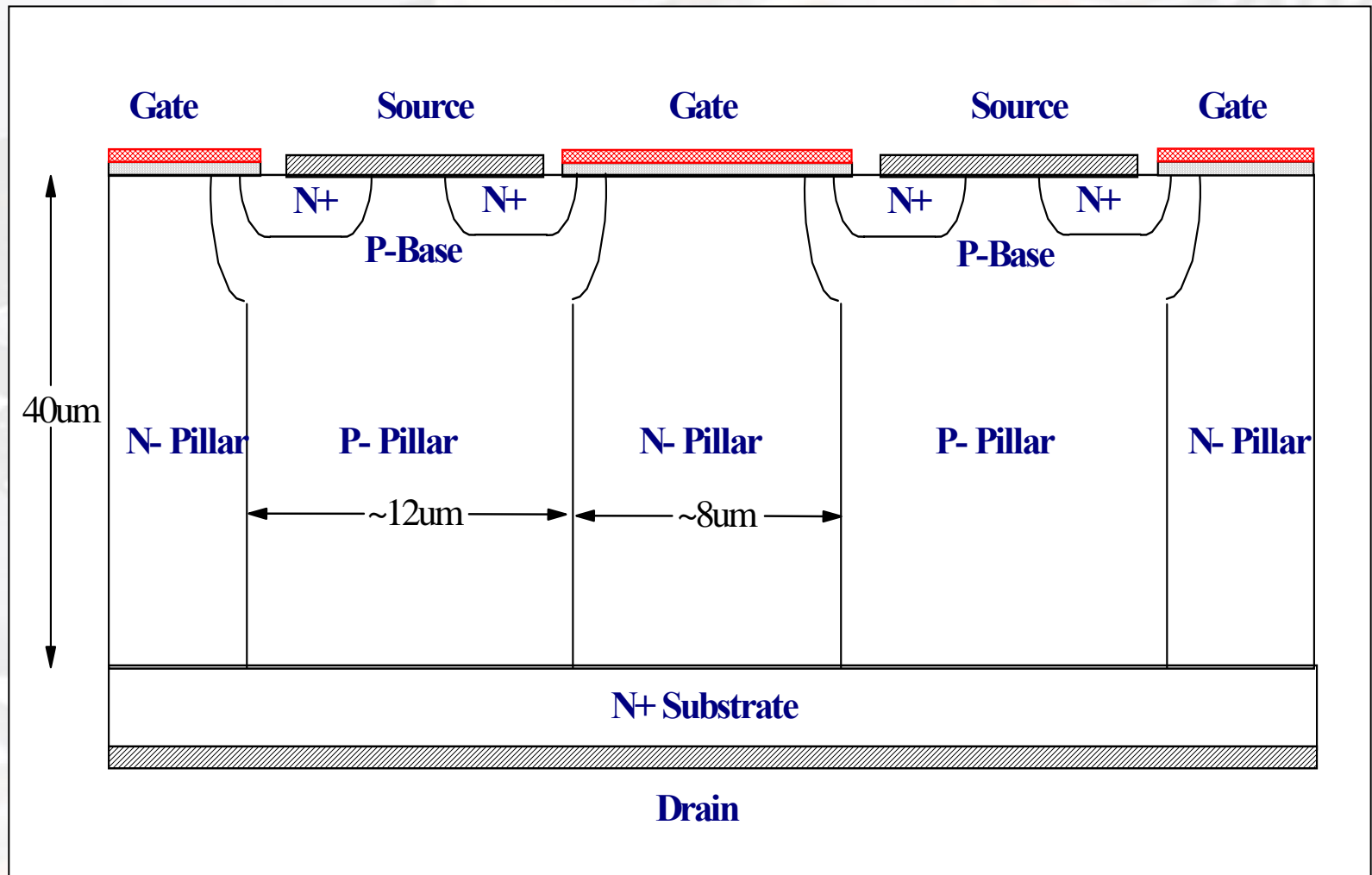
Figure of Merit Trend

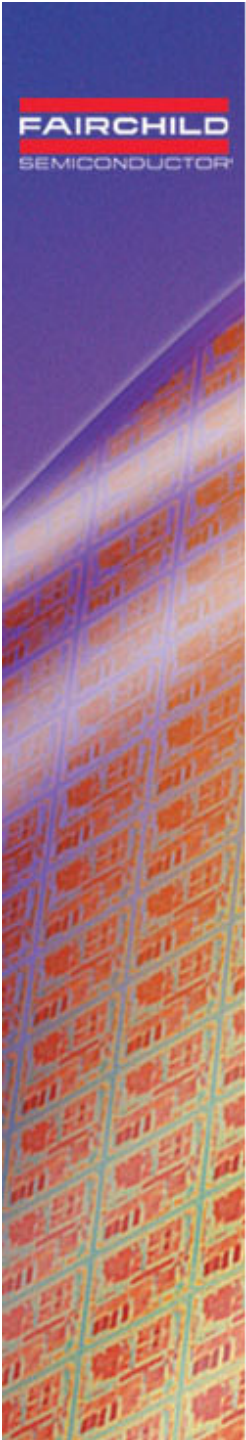
$R_{on} * Q_{gd}$

Figure of Merit vs. Time

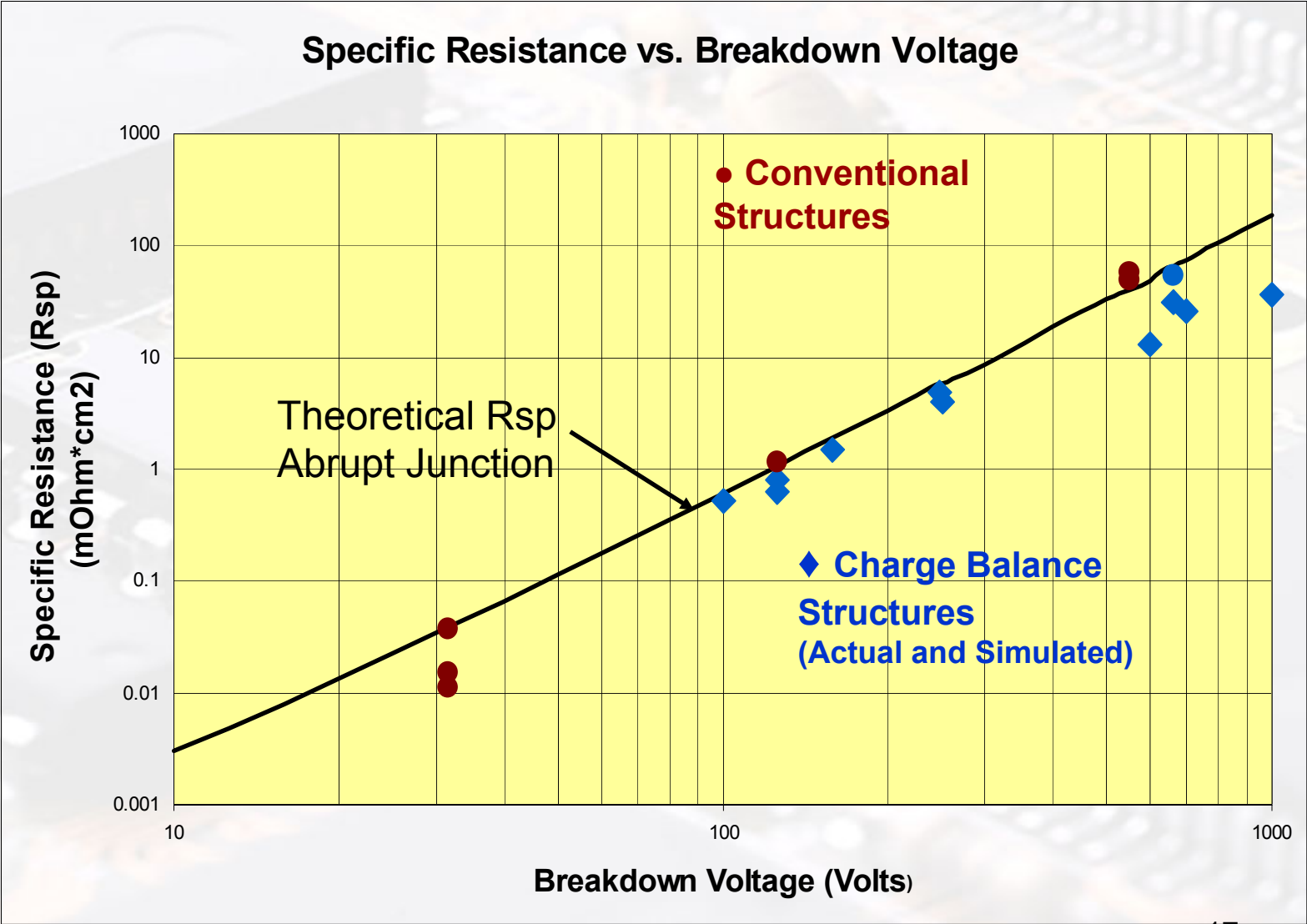


Advanced Structures: Charge Balance MOSFET





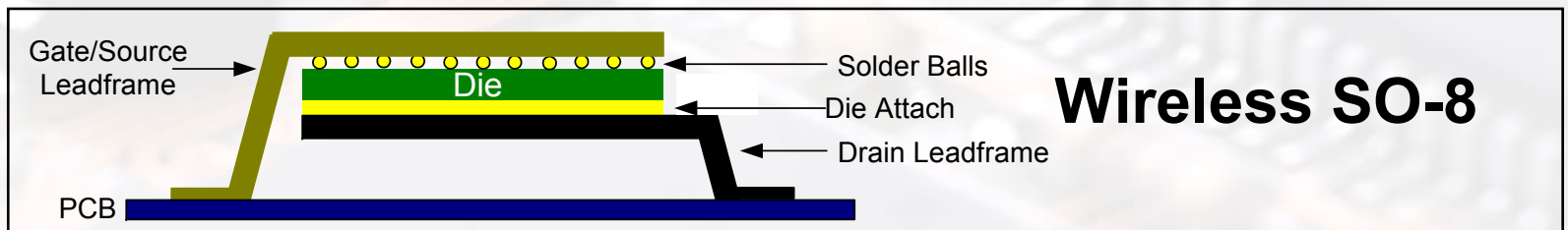
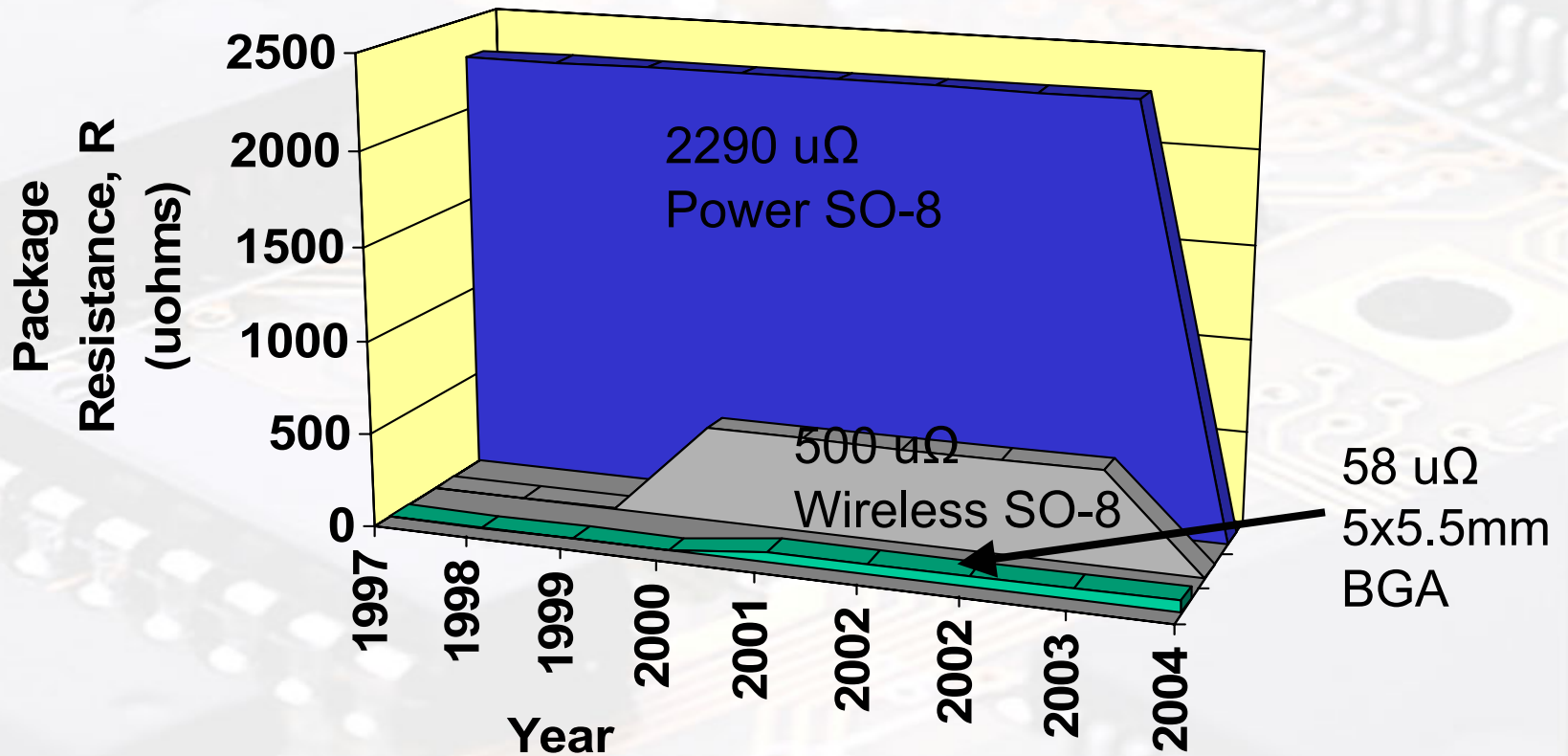
Advanced Structures vs. Theoretical Resistance



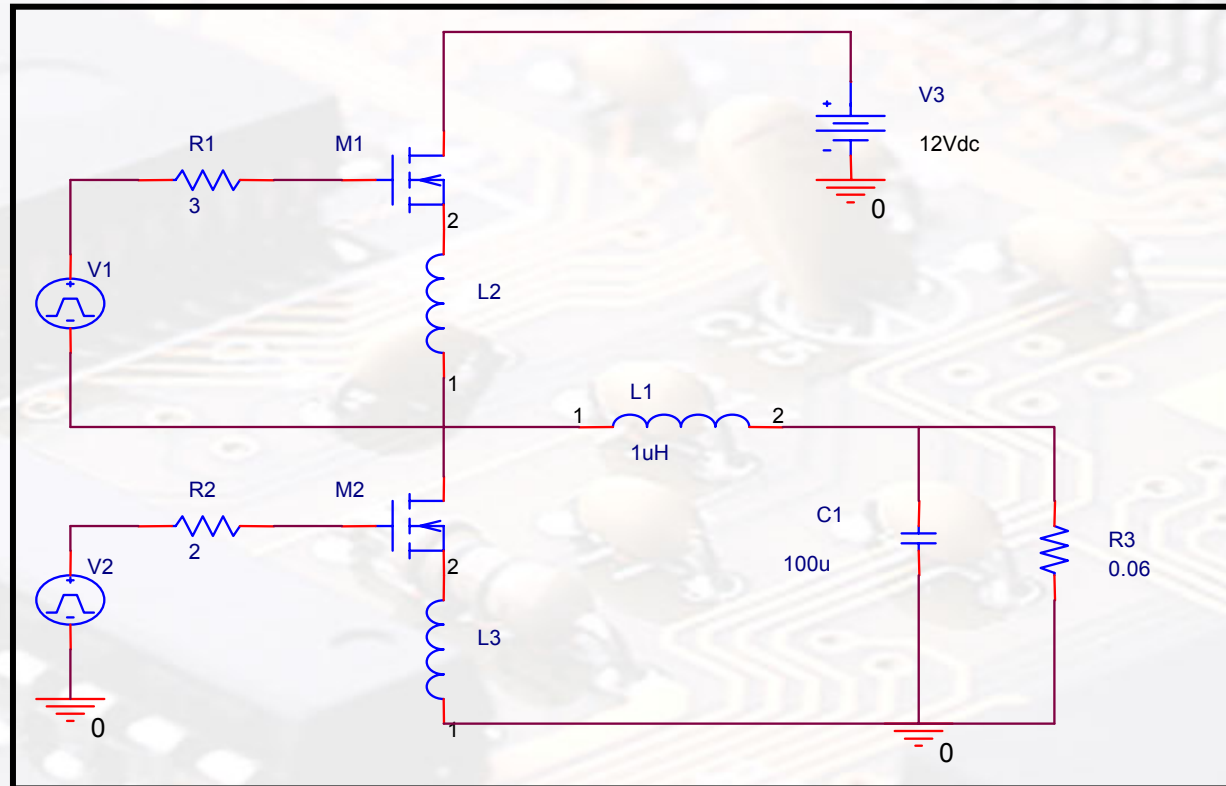
The Power Switch: Beyond the Silicon

- Significant improvements have been achieved as **Silicon advancements**
- Rds(on)
- Gate Charge
- Advancements continue in these areas
- **Package advancements** have also been achieved
- On-state losses:
 - Package resistance
- Switching losses:
 - Package inductance
 - Becoming significant in converter performance as switching frequency increases

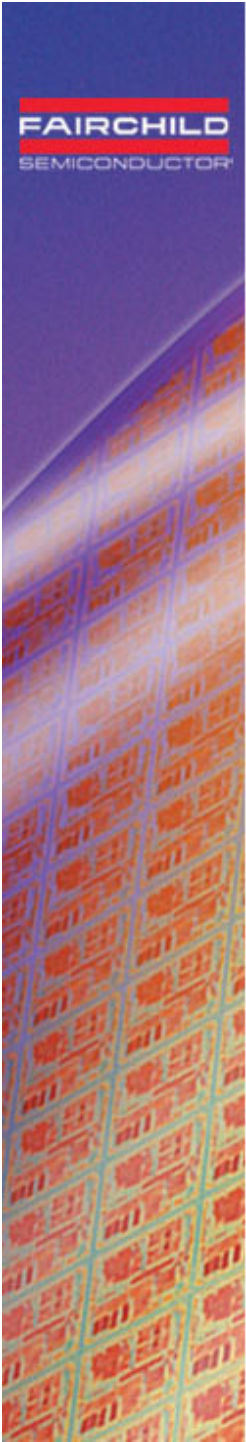
Package Resistance Trend



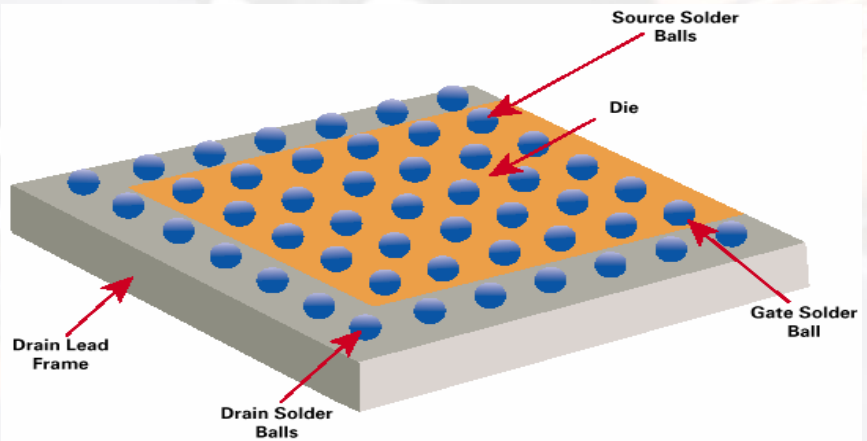
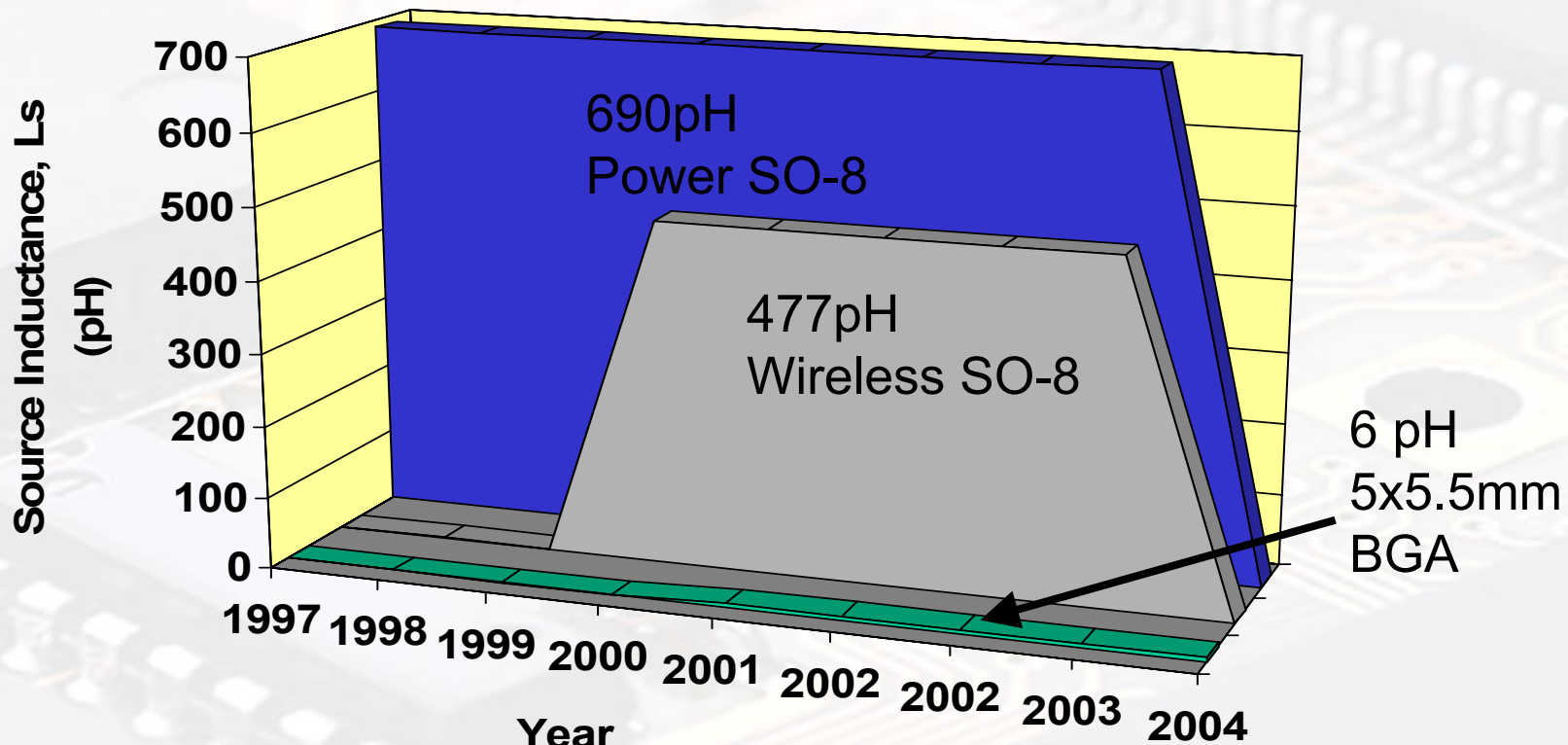
Parasitic Source Inductance



- In HS MOSFET, L_s controls the rise and fall of the Drain current
- In LS MOSFET, may cause ground bounce
- In all cases will cause increased power dissipation



Package Source Inductance



BGA Package

Summary

- The progression towards the Ideal Power Switch continues
- Specific Resistance and the Figure of Merit have decreased by over 70 percent in the past 8 years
- Significant advancements have been made in packages for reduced resistance, for improved static performance, and inductance improvements, for the dynamic switching parameters
- With these advancements of the power switch performance, the voltage regulator module has improved in both performance and cost effectiveness
- Continued advancements in both the active switch as well as packaging will enable even greater power density





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