



Integration Challenges in DC/DC Converters

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Texas Instruments

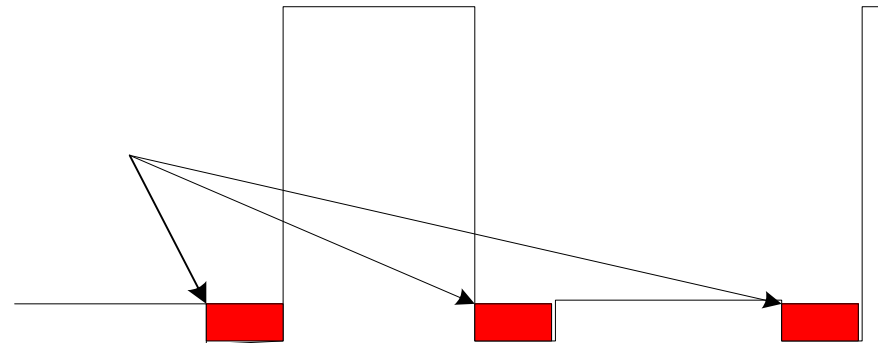
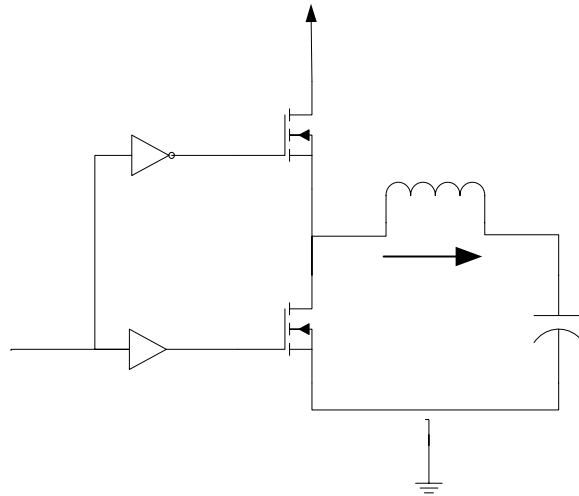


Current Products

- Texas Instruments, Intersil, Maxim, International Rectifier
 - High Performance Controllers
 - 1% Reference
 - High Switching Frequencies
 - High Performance Op Amps
 - Integrated Synchronous Rectification
 - 3A – 15A? Output
 - MOSFET Output Devices
 - Thermally enhanced packaging
 - Monolithic and Hybrid Devices



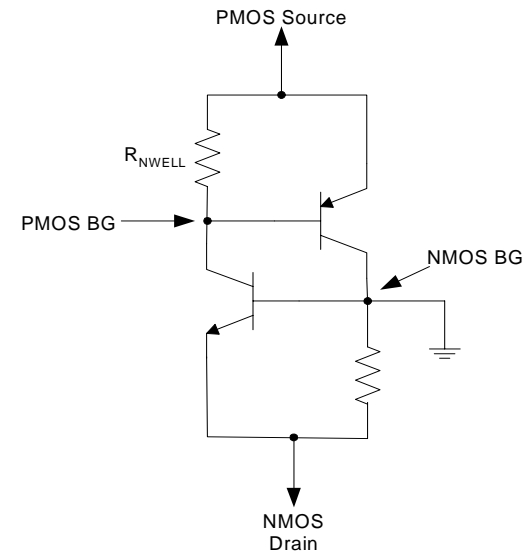
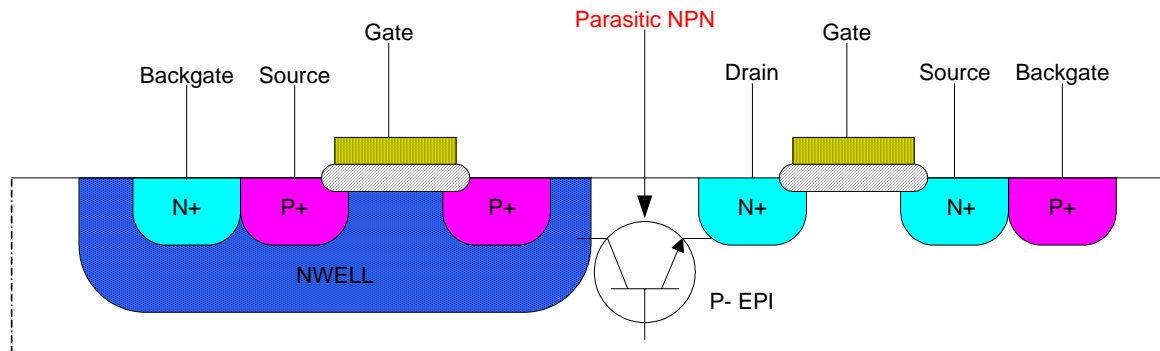
Diode Conduction



- Efficiency loss.
- Minimize dead-time.
- What effect on circuit?



Minority Carrier Injection

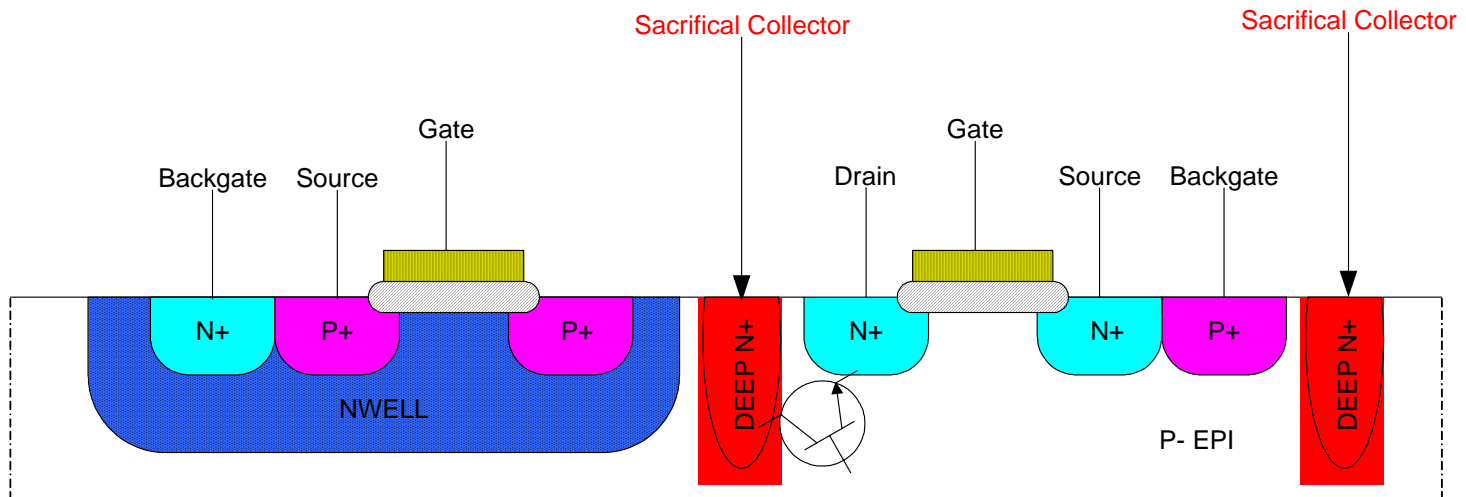


- Latchup

- Formed by parasitic devices bipolar devices in CMOS technology
- Potential to destroy IC



Minority Carrier Injection

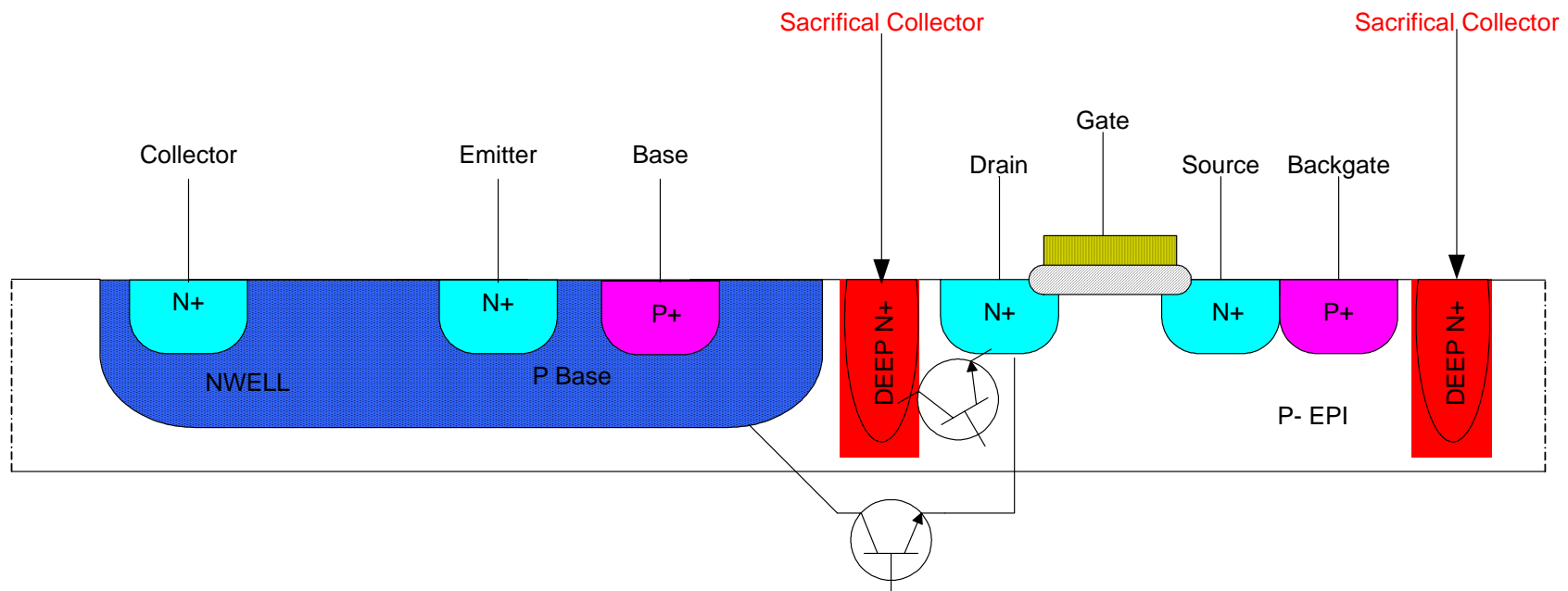


- Latchup prevention

- Utilize sacrificial collector to limit current collected by PMOS source
- Does not collect 100% of minority carriers; Latchup still a concern
- Still have substrate injection that affects circuit performance



Minority Carrier Injection



- Circuit performance issues

- Small current significantly affects NPN's and PNP's

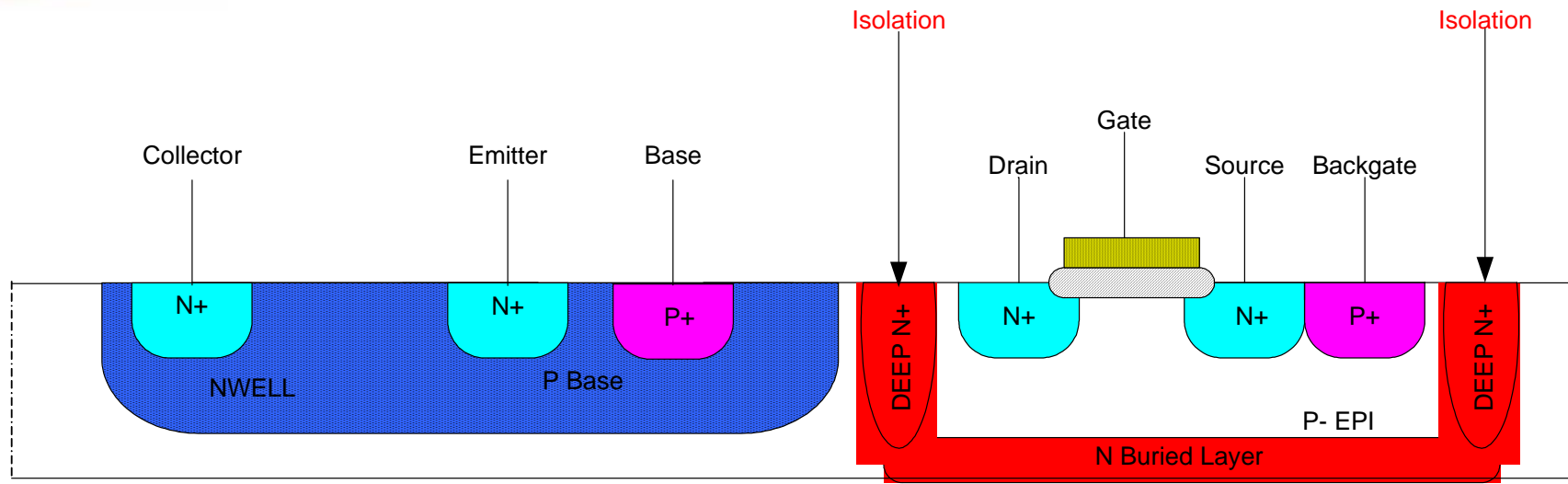
- o Collector of NPN acts as collector for minority carriers (figure above)

- o Base of PNP acts as collector for minority carriers

- Small current affects drain/source of NMOS devices



Minority Carrier Injection

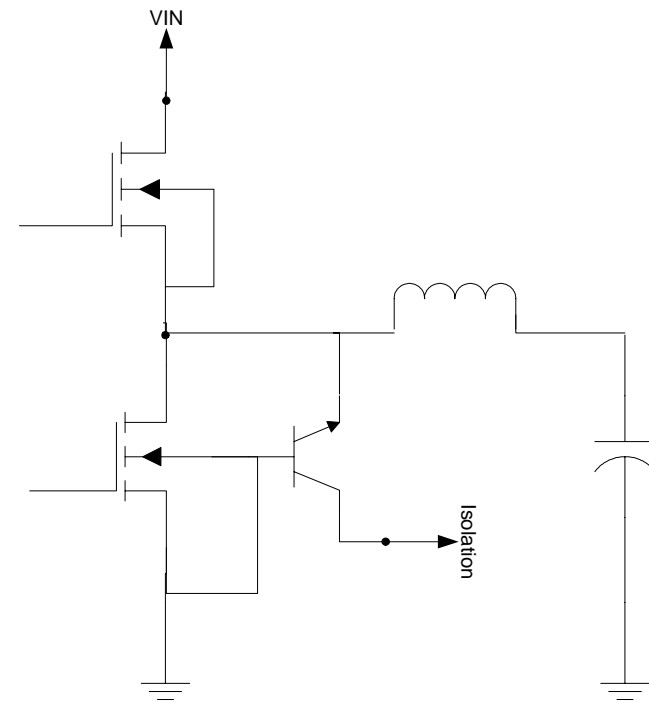


- Utilize buried layer to further reduce substrate injection
 - Greatly reduces injected current
 - Must watch punch-thru from drain to isolation
 - Resistance in buried layer must be minimized in order to kill/limit substrate PNP



Minority Carrier Injection

- Where to connect isolation?
 - Connect isolation to V_{in}
 - o Better collection of minority carriers
 - o Reduces efficiency of converter
 - Connect isolation to GND
 - o Adequate collection of minority carriers
 - o Does not impact efficiency



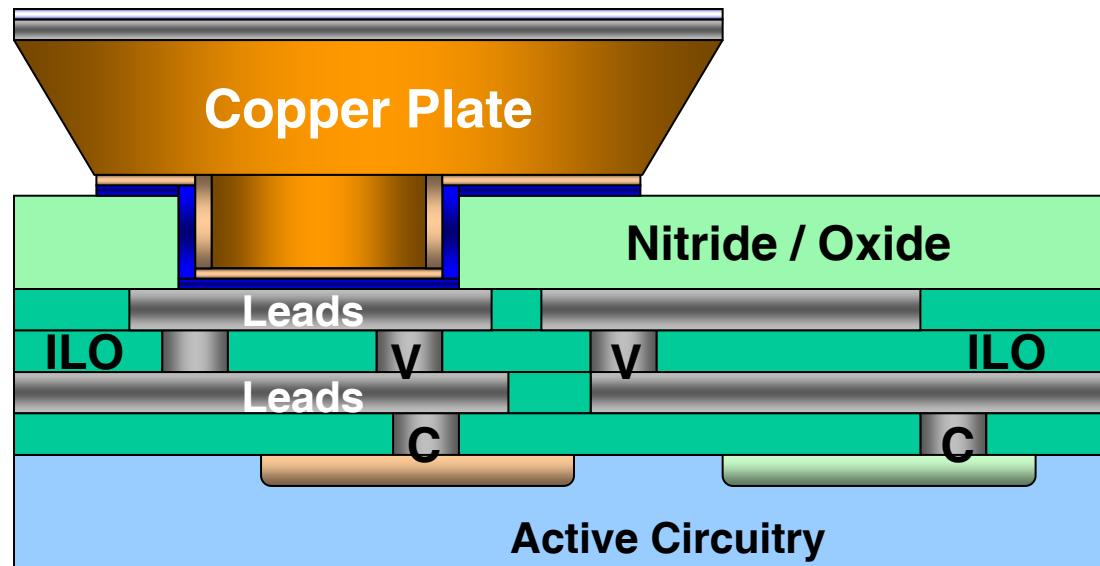


Minority Carrier Injection

- Circuit design considerations
 - NPN's and PNP's
 - o Increase collector currents (NPN)
 - o Balanced circuits where applicable
 - o Avoid if possible
 - NMOS
 - o Increase source/drain currents
 - o Balanced circuits where applicable
 - o Isolated backgate if possible
- Floorplanning
 - Keep sensitive analog circuits away from power devices
 - Placement of low-side FET critical



Low R_{dson} FETs

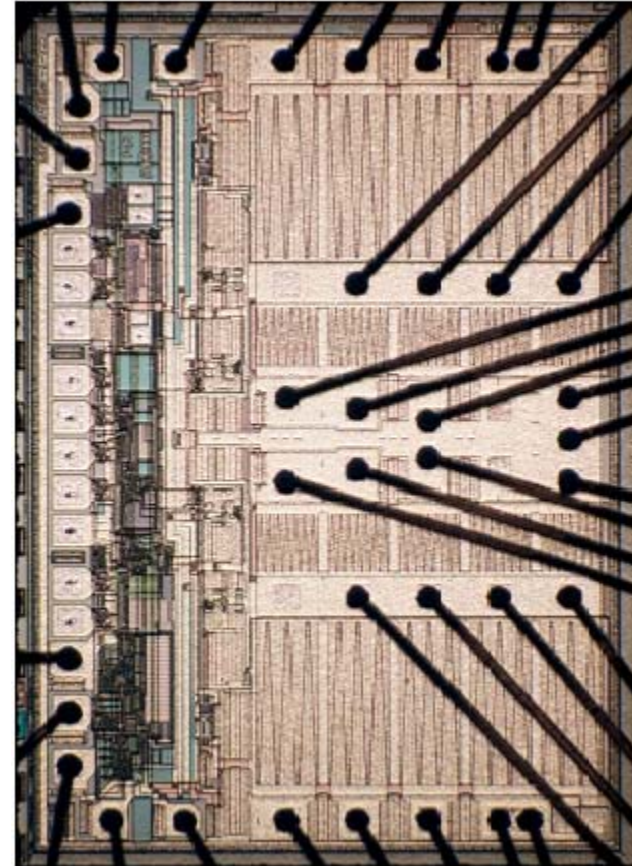


- Thick metallization
 - o Reduces lateral debiasing
 - o Minimizes contribution of metal resistance
 - o Thermal performance improvement



Low R_{dson} FETs

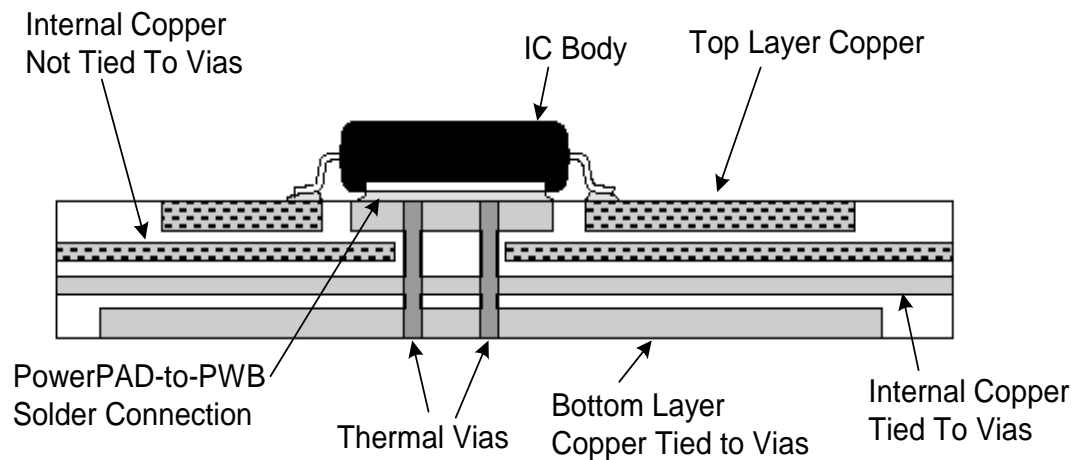
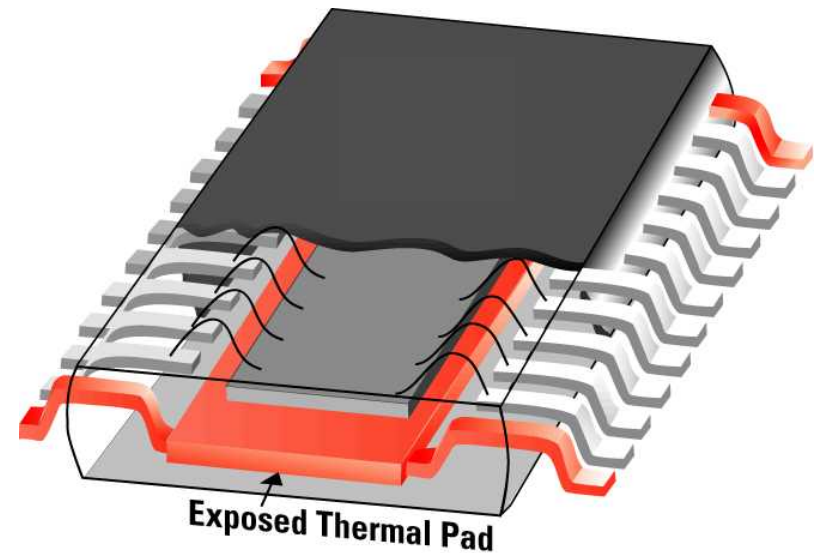
- Unique Bonding
 - Minimize contribution of metal resistance
 - Reduce lateral debiasing
 - Does not jeopardize floorplan





Thermal Performance

- Package Characteristics
 - Small size
 - Good thermal performance
 - No heat sinks
- Exposed Thermal Pad Packages
 - SOIC, TSSOP, QFN





Thermal Performance

- How much better?

TSSOP 24	PowerPAD™	Standard Package
Theta _{JA}	30.13 C/W	128.44 C/W
Theta _{JC}	0.92 C/W	14.83 C/W
Power Handling (150C junction and 80C ambient)	2.32 W	0.55 W
Junction Temp (0.5W operation and 80C ambient)	95 C	144 C



Future Trends and Challenges

- Higher currents, higher efficiencies
 - Lower R_{dson} FETs
 - Minority carrier injection
 - Minimal gate charge loss
- Solution size
 - Higher frequencies
 - Lower R_{sp} FETs
 - Smaller packaging
- Thermal performance
 - Heat from PWP
 - Heat from top
 - FET as heat sink
 - Heat from metal and bond wires