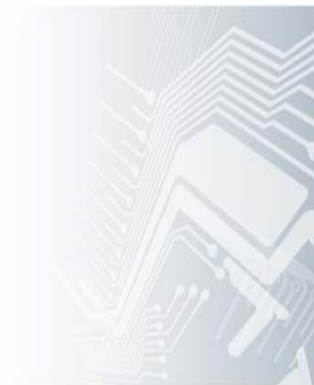


# Power Supply Trends in ASIC Products



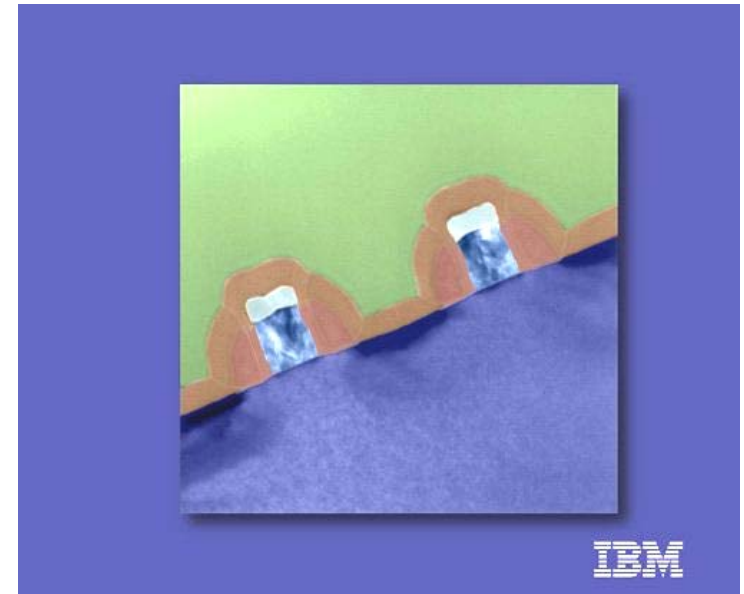
Paul S. Zuchowski  
Charles A. Kilmer  
Thomas R. Bednar

# Agenda

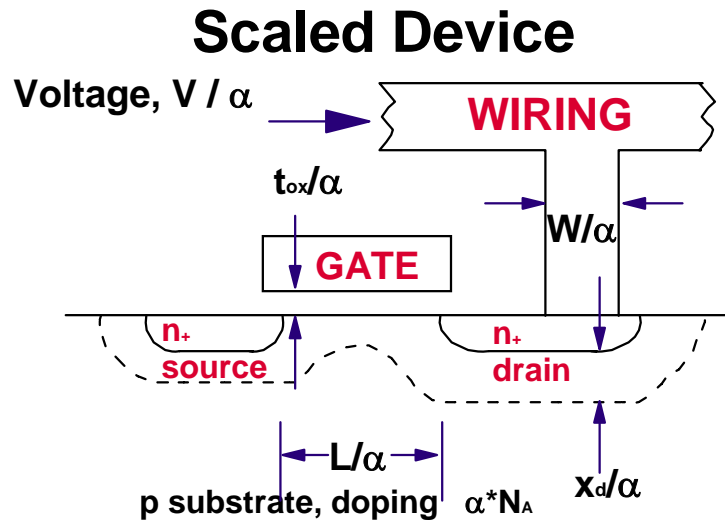
- CMOS Scaling Review
- The Leakage Problem
- On-Chip Power-Supply Requirements
  - Delay Sensitivity to  $\Delta V_{DD}$
  - Historical and Projected Supply-Voltage Requirements
- Power Supply Noise-Transfer Functions
  - Card to Chip
  - Chip to Card

# Classical Silicon Technology Scaling

- Lithography advances double circuit density every generation (~18 months)
- Technology scaling allows transistor drive current to be maintained at lower voltages and for smaller device sizes
  - Shorter channels and thinner device oxides improve transconductance
  - Reduced per-circuit capacitance and voltage swing result in performance increases generation to generation
- Switching (active) power per unit area remains relatively constant
  - Capacitance density increase is offset by voltage reduction in the power equation ( $CV^2f$ )
- Increases in power density driven by frequency increases are supported by improved product architectures



# Technology Innovation: Classical Scaling Has Ended

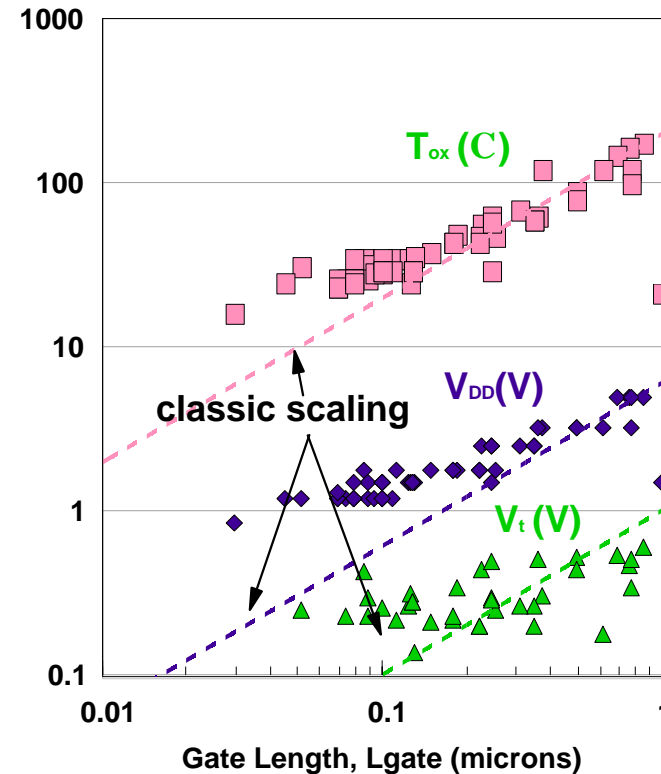


#### Scaling:

Voltage:	$V / \alpha$
Oxide:	$t_{ox} / \alpha$
Wire width:	$W / \alpha$
Gate width:	$L / \alpha$
Diffusion:	$x_d / \alpha$
Substrate:	$\alpha * N_A$

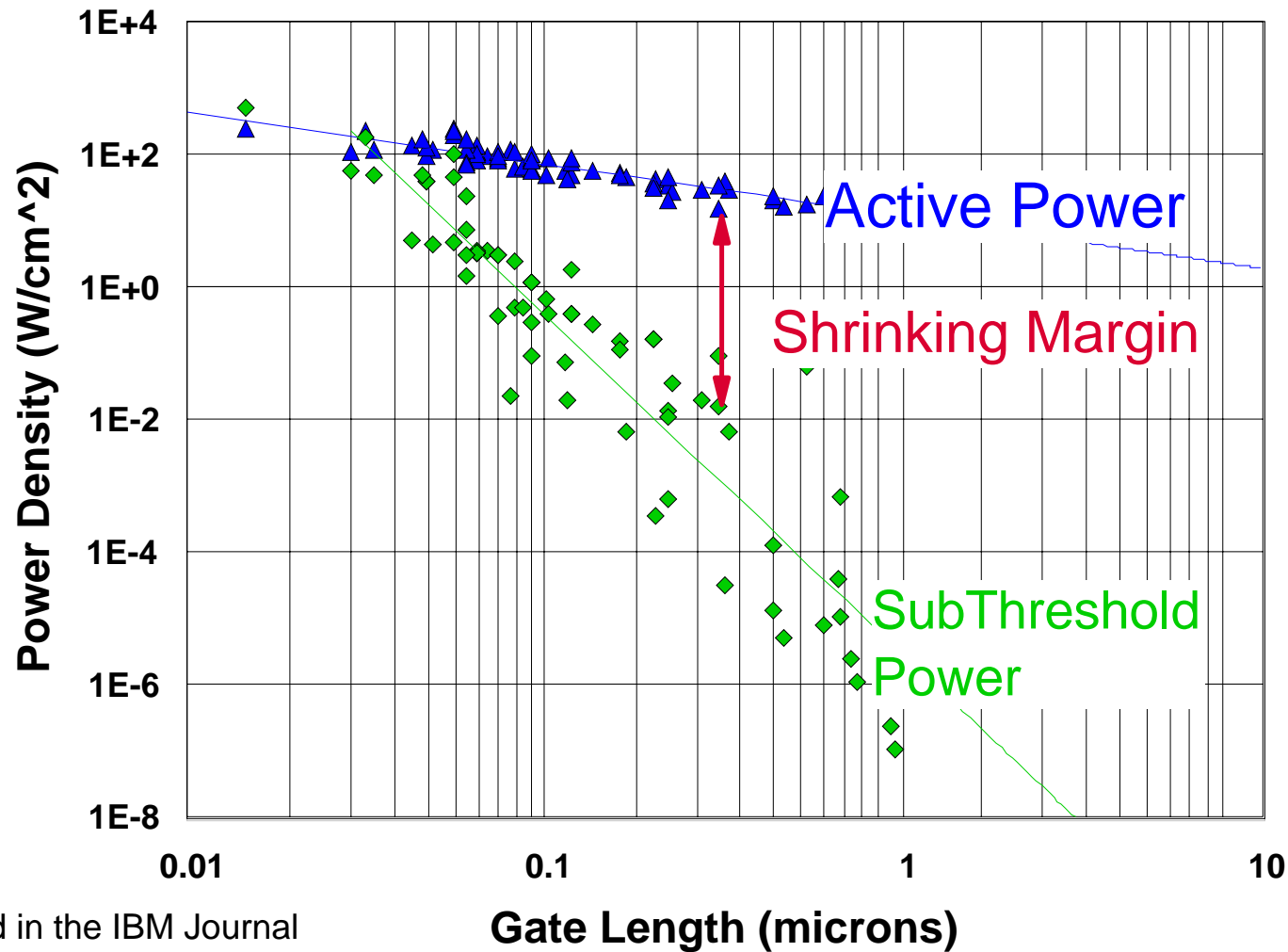
#### Results:

Higher Density:	$\sim \alpha^2$
Higher Speed:	$\sim \alpha$
Power/ckt:	$\sim 1 / \alpha^2$
Power Density:	$\sim \text{Constant}$



- Why deviate from "ideal" scaling?
  - Unacceptable gate leakage/reliability
  - Additional performance at higher voltages
- What is the consequence of this deviation?
  - A dramatic rise in power density

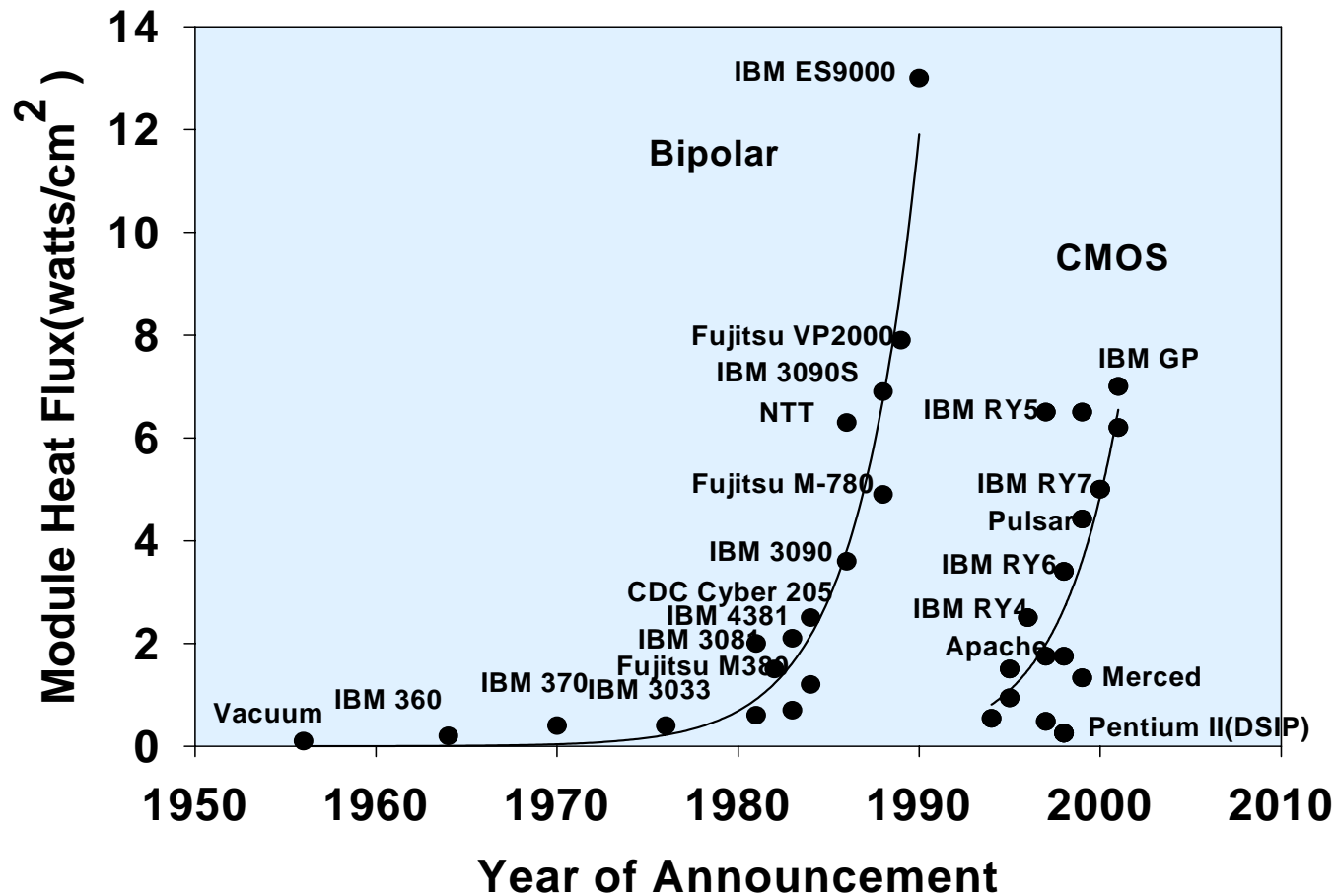
# Leakage Power Density Increasing



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of Research and Development,  
No. 2/3 March/May 2002.  
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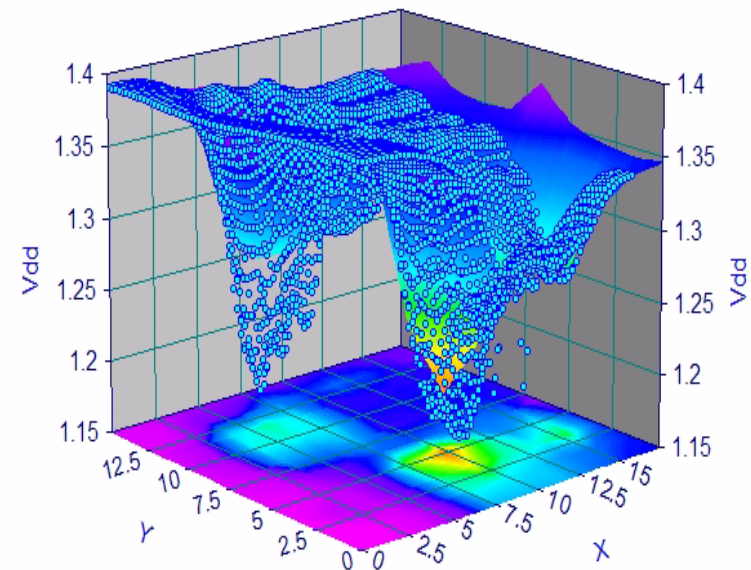
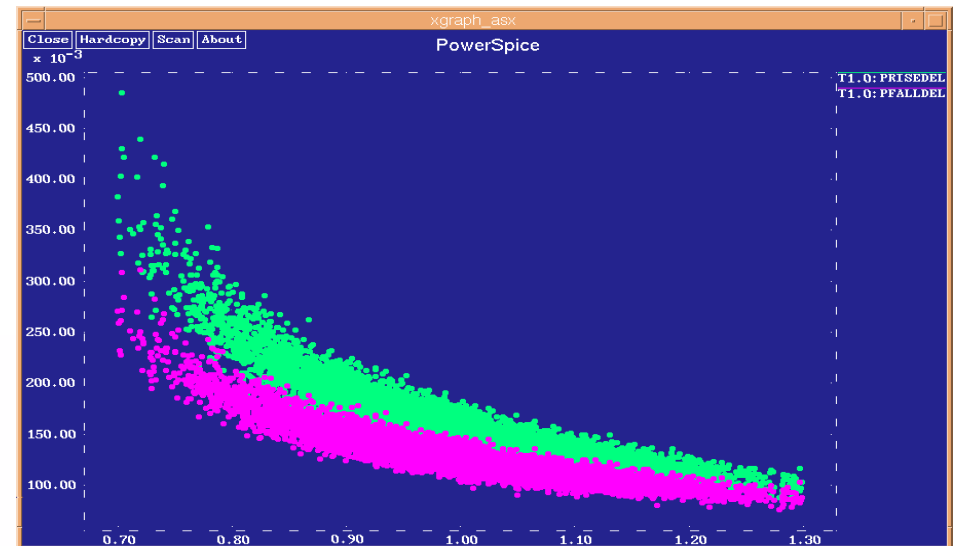
# Result: Unacceptable Escalation in CMOS Power Density

## Heat Flux Explosion



# Supply Sensitivity

- Scaling reduces  $V_{DD}$  headroom -> we are operating on a steeper portion of the delay versus  $V_{DD}$  curve
- As  $V_{DD}$  supply values drop and power densities increase, the current per unit area increases -> IR drop becomes more of an issue
- At higher frequencies, off-chip decoupling can't keep up with the instantaneous current demands of the circuits -> instantaneous voltage drop must be analyzed



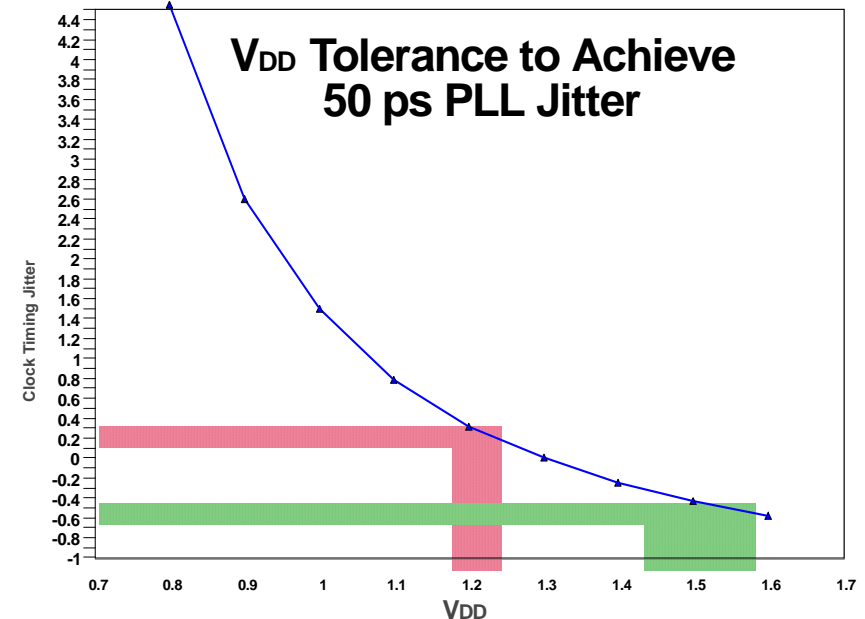
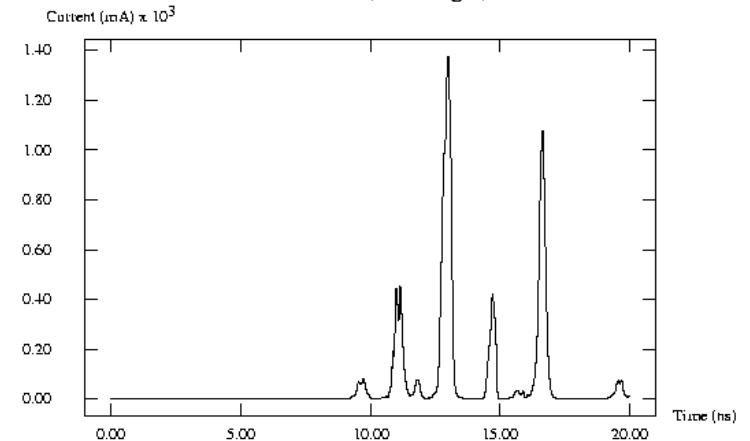
# Embedded CAM

## • TCAM

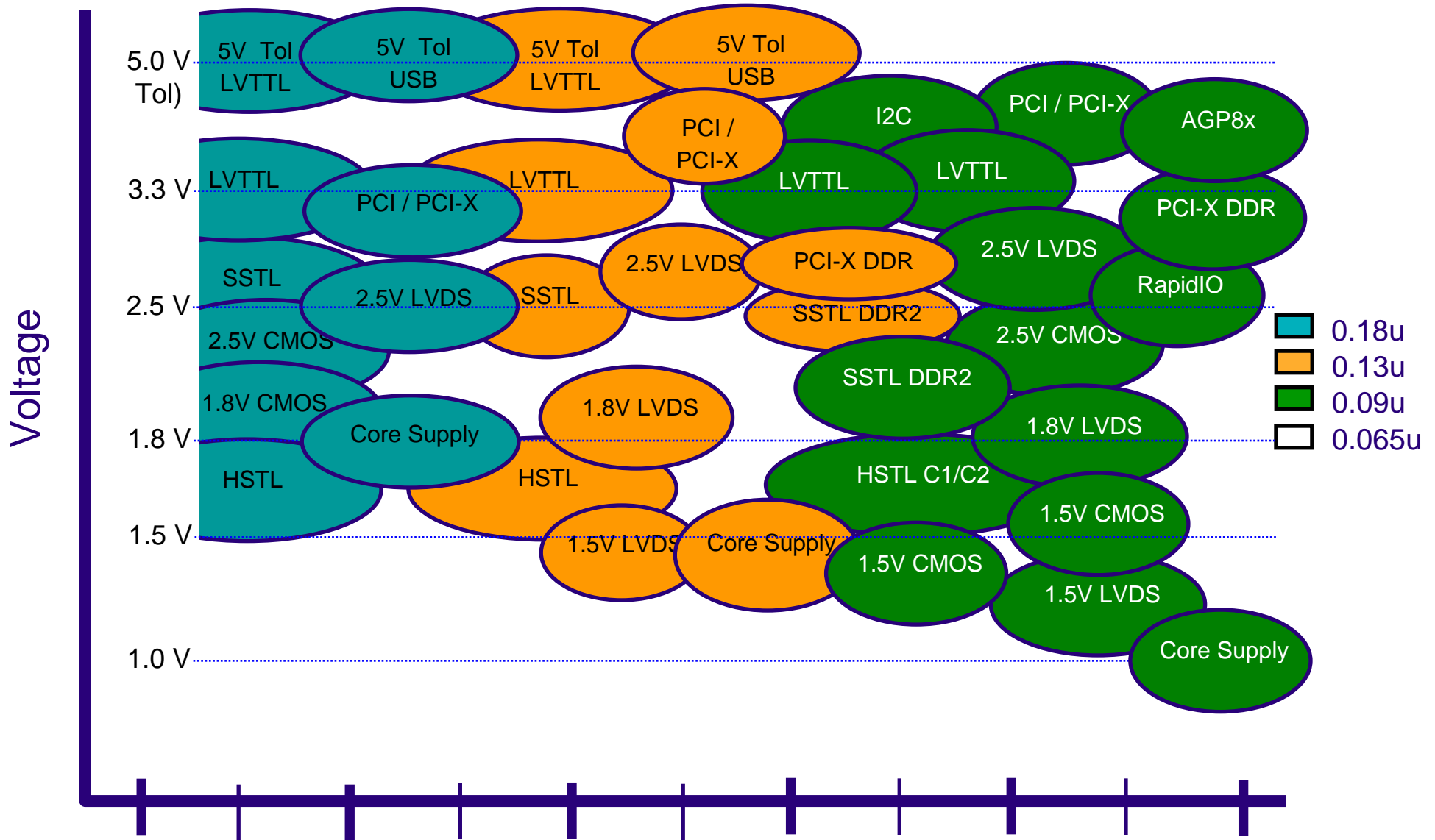
- Entries stored in array
- Two SRAM cells + per bit comparator
  - “1” / “0” / Care / Don’t Care
- Searches across all entries in single cycle
- Up to 15 macros per chip
- 250 MHz search and match-line operation
- Maximum currents up to 20A
- Typically PLL required to align output timing
- Separate  $V_{DD}$  power supply island for macro
  - Lower  $V_{DD}$  to reduce power
  - Isolation from sensitive PLL circuits

For 50-ps jitter at 1.5-V  $V_{DD}$ , tolerance is +/- 75 mV: at 1.2 V, tolerance goes to +/- 30 mV

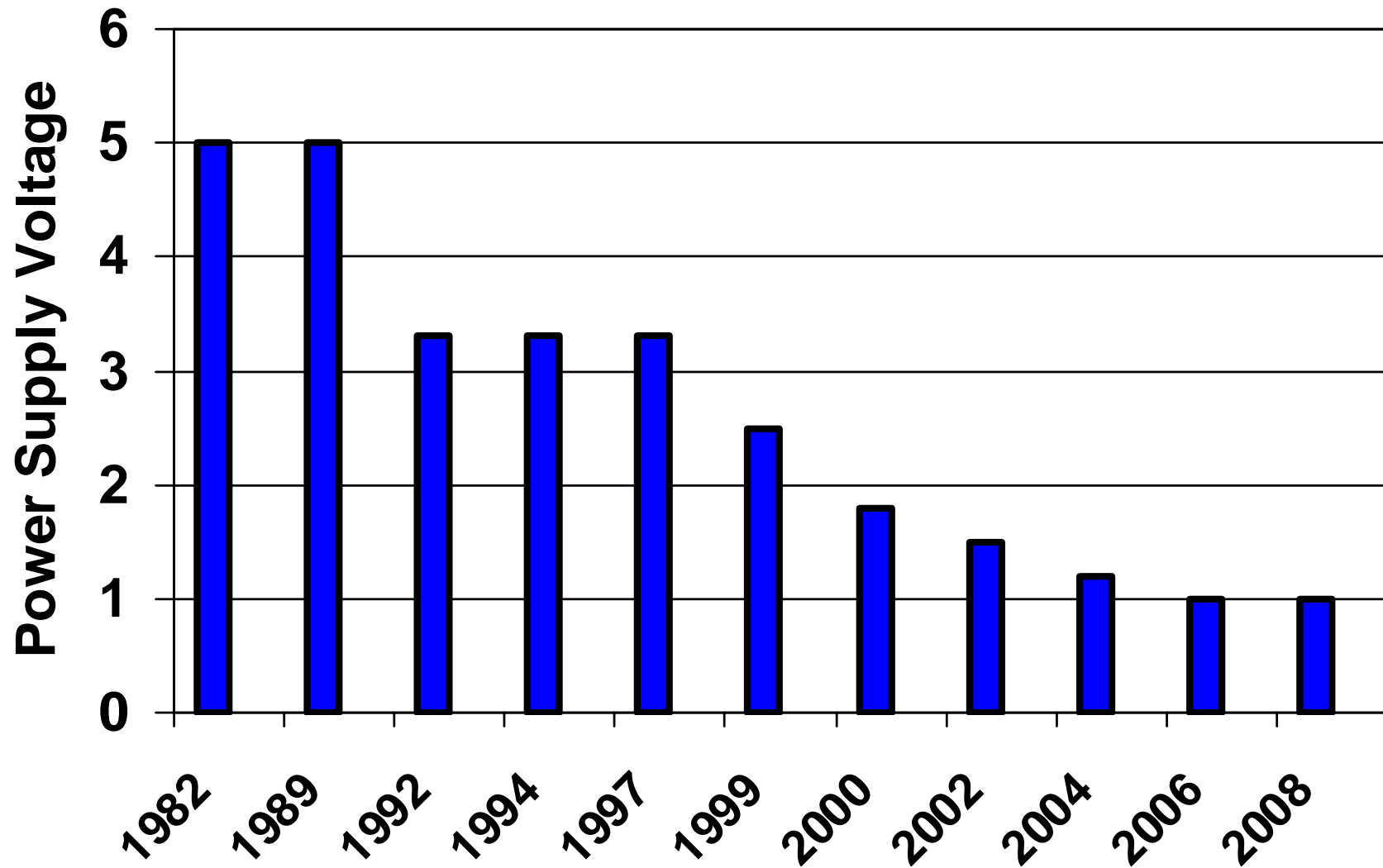
1024X52: 1.4V, 105 degC, WC



# Legacy I/O Requirements Propagate Voltage Levels

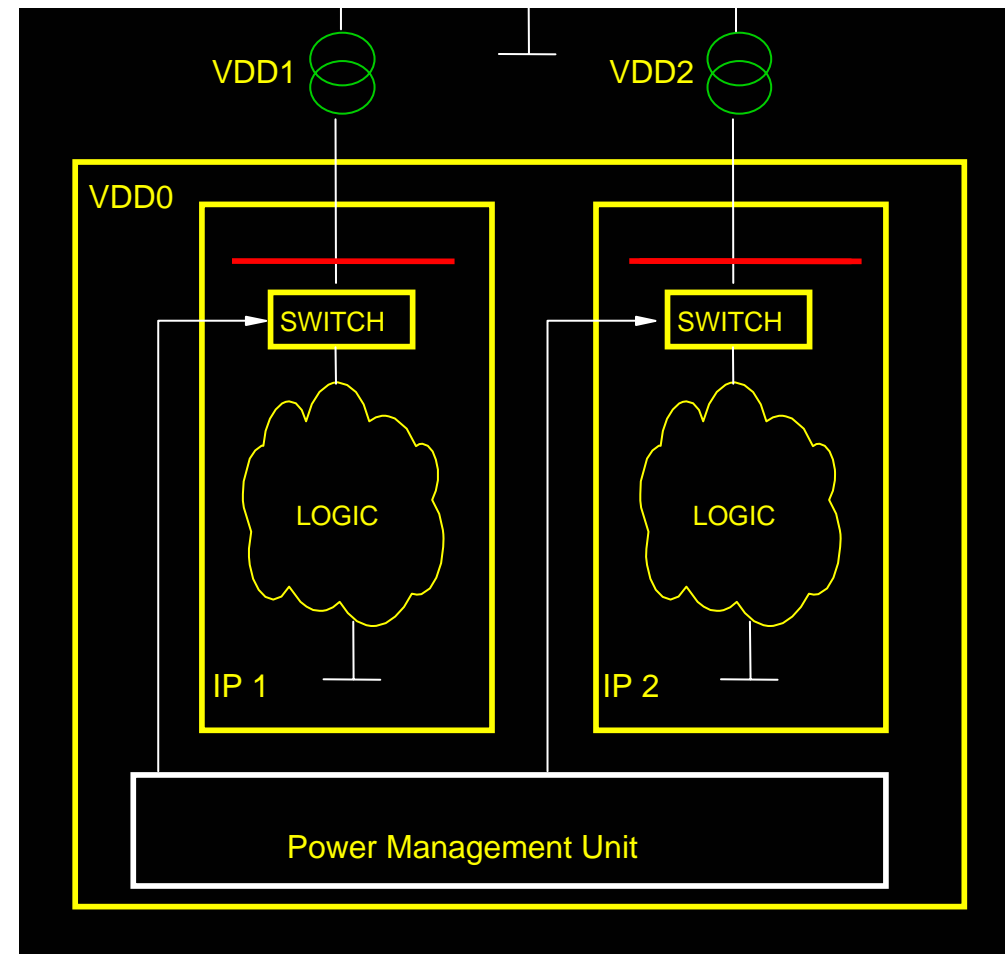


# Primary ASIC Power-Supply Trend



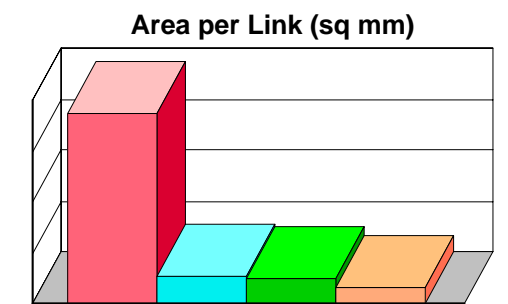
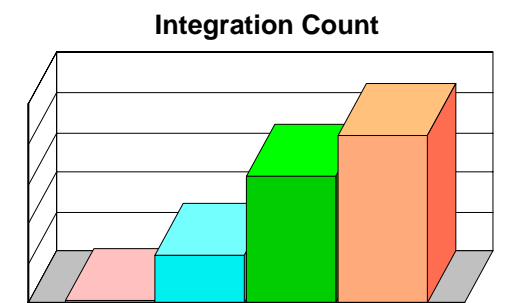
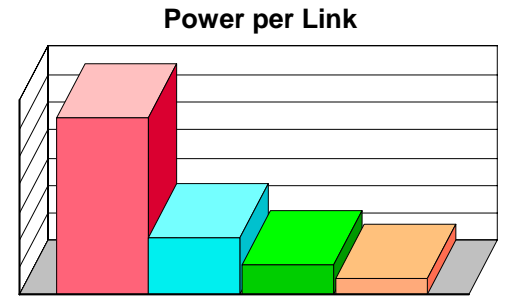
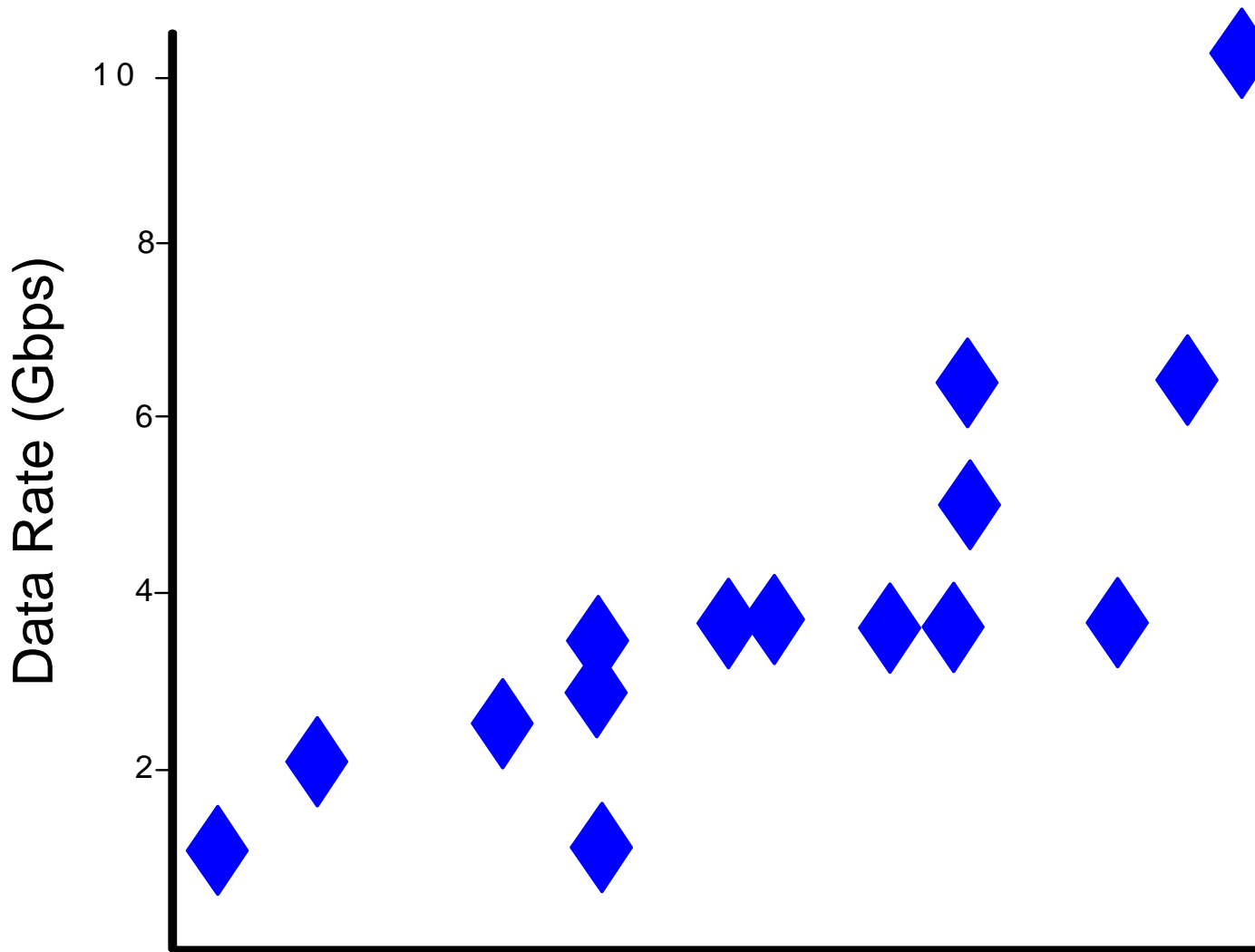
# Voltage Islands and Power Domains

- **Voltage islands**
  - Areas on chip supplied through separate, dedicated power feed
- **Power domains**
  - Areas within an island fed by same  $V_{DD}$  source but independently controlled via intra-island header switches
- **Simple concepts ... complex methodology and design tools**

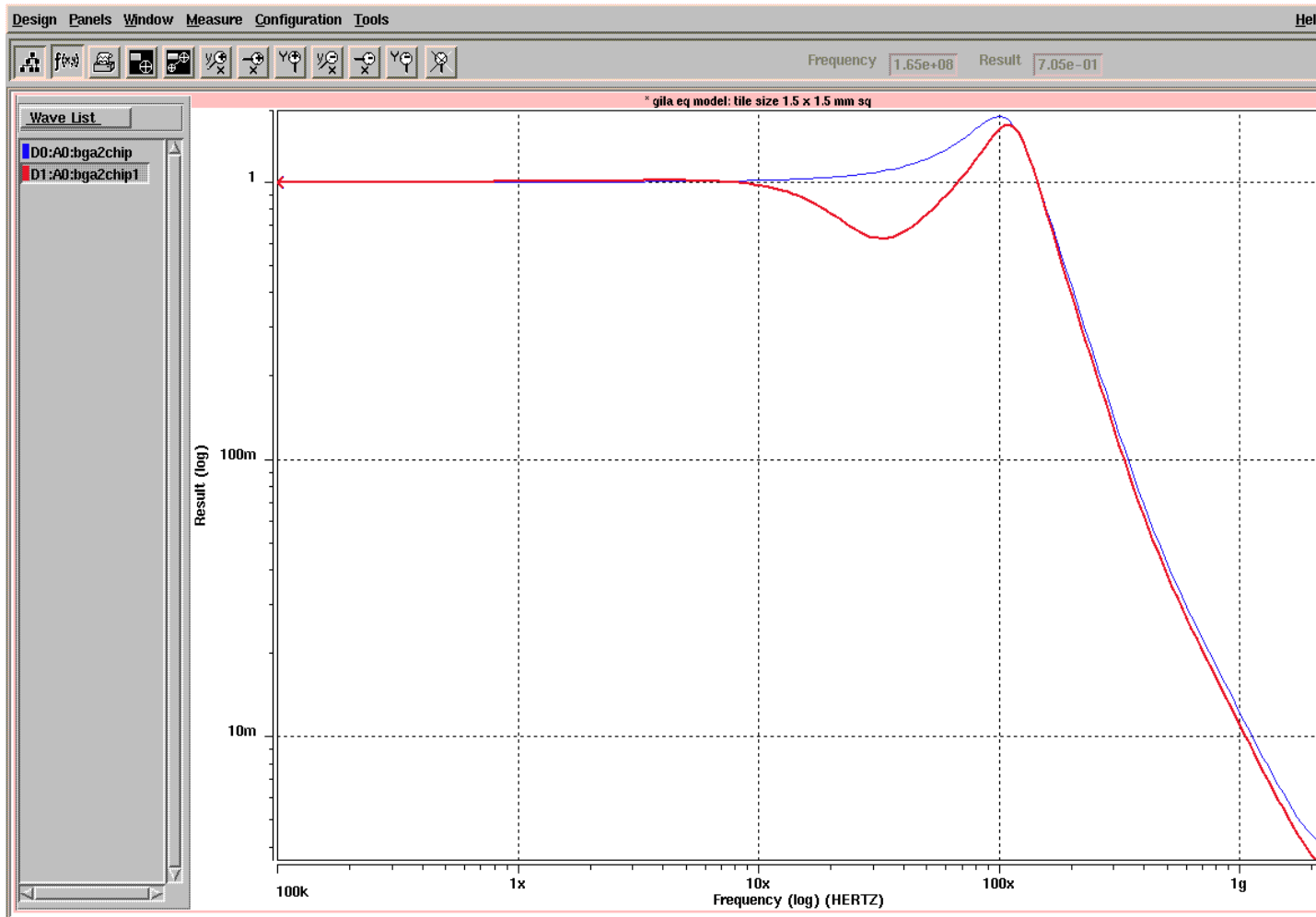


# High-Speed Serial Interface Directions

- Skyrocketing performance with higher levels of integration, while reducing power

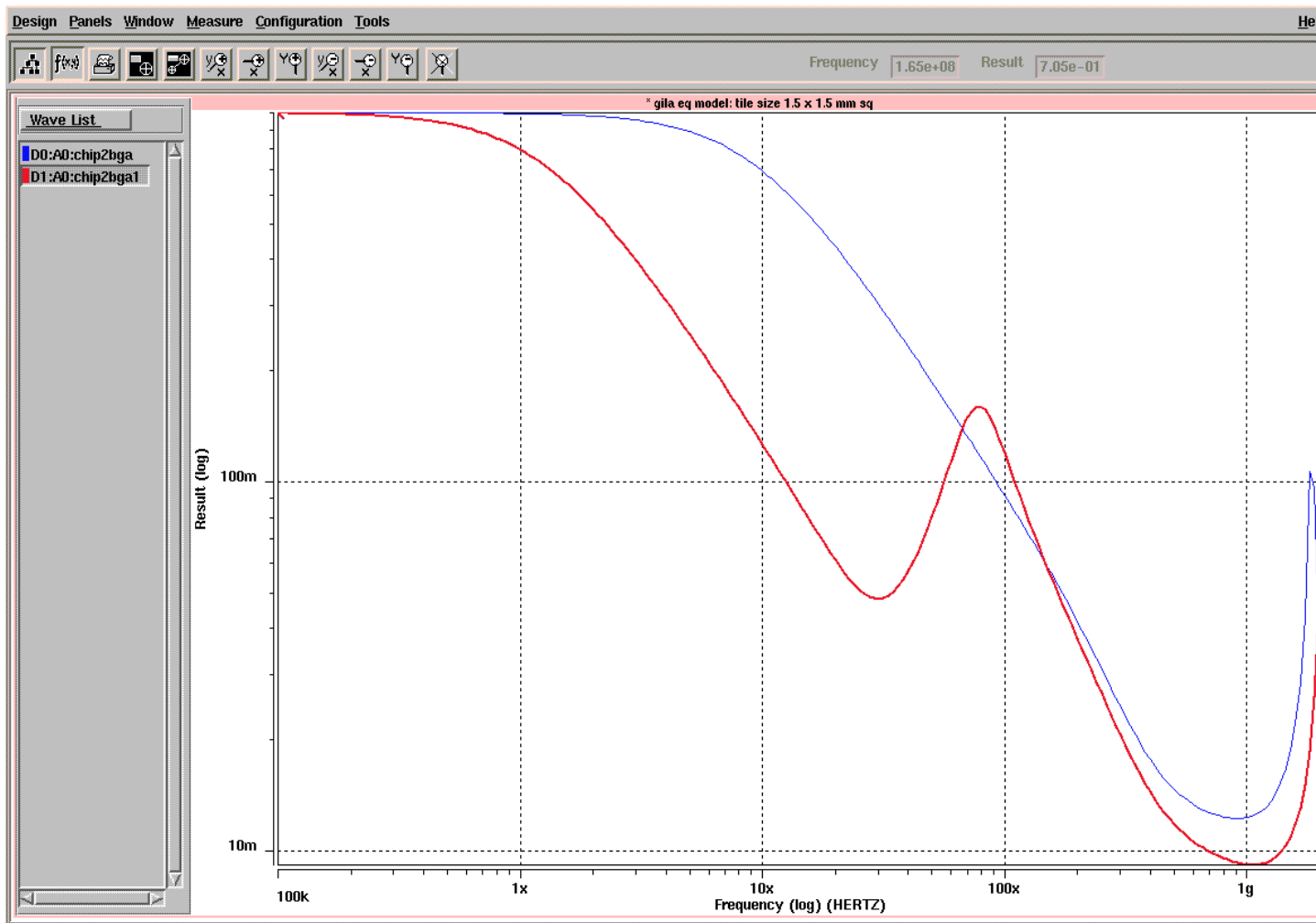


# AC Transfer Function – Board to Chip



Courtesy of: Eric Tremble, Tim Budell and Nanju Na

# AC Transfer Function – Chip to Board



- Without package decaps
- With package decaps

Courtesy of: Eric Tremble, Tim Budell and Nanju Na

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- Nanju Na

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